think SPEED think GiDEL™

High Speed Multi-User ASIC/SoC Prototyping system

Technical Resource Document

Date: August 23, 2010

U.S.A. 1600 Wyatt Drive, Suite 1 Santa Clara, CA 95054 Tel: 1 - 408 - 969 – 0389 Fax: 1 - 866 - 615 – 6810
Email: sales_usa@gidel.com
Worldwide. 2 Ha'ilan, Or Akiva 30600, Israel Tel: +972-4-610-2500 Fax: +972-4-610-2501
Email: sales_eu@gidel.com

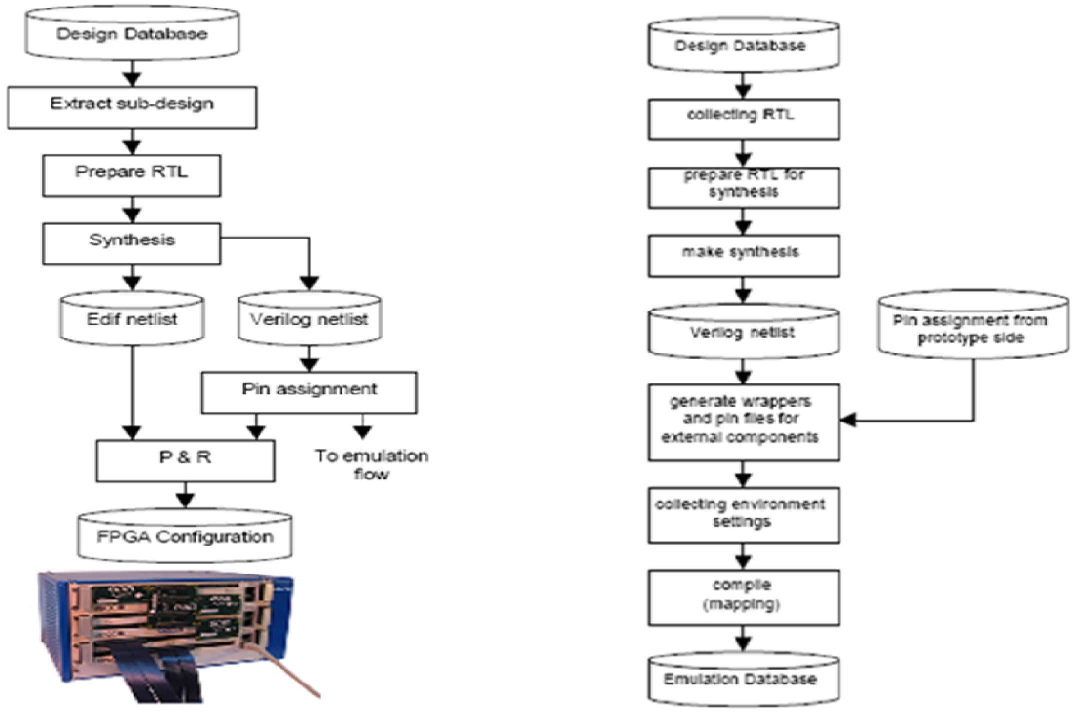
About GiDEL

GiDEL has become one of the market leaders as a company that continuously provides cutting-edge reconfigurable technology utilizing FPGAs. The PROC families of reconfigurable PROCessors are used for (1) for SoC and ASIC verification, (2) as COTS (Commercial Off-The-Shelf) acquisition and accelerator boards, and (3) to validate complex algorithms.

Background

As the size of the verification task for SoCs continues to balloon, more verification teams are turning to some sort of hardware emulation to increase the number of cycles they can run. But emulation brings its own hard decisions. Big-iron hardware emulators give nearly as much control and observability as simulation. But they are relatively slow and low in capacity, and they are beyond the budgets of most teams. **FPGA prototypes—often on boards designed by the SoC team itself—are far less expensive, but they are design projects in their own right. Also, they tend to offer little control or visibility beyond breakpoints and hooks you put into the RTL yourself with a resynthesis and remapping**

Design Flow Prototyping Vs Emulation



Prototyping Design Flow

Emulation Design Flow

In many cases, it is necessary to verify the design "at-speed." Take an example of a video processing chip part of the verification may involve evaluating the subjective quality of the video output stream. The solution is to create a hardware prototype of the ASIC design using one or more FPGAs. One important benefit of this approach is the ability to run external interfaces at full speed. As a functionally equivalent version of the ASIC, FPGA-based prototypes enable both chip and system-level testing. In addition to providing real-time simulation speeds in the order of 10 MHz to 100 MHz, such prototypes are relatively inexpensive, thereby allowing them to be provided to multiple developers and also to be deployed to multiple development sites. **Due to their superior performance and affordability, FPGA-based rapid prototypes are ideal as pre-silicon software development platforms.**

Multi-User ASIC/SoC Prototyping System

GiDEL's PROC_SoC system meets the increasing verification needs of large SoC designs and system software development. In particular, the PROC_SoC is a high speed verification system for designs with complex structures requiring large amounts of interconnect between the FPGAs.

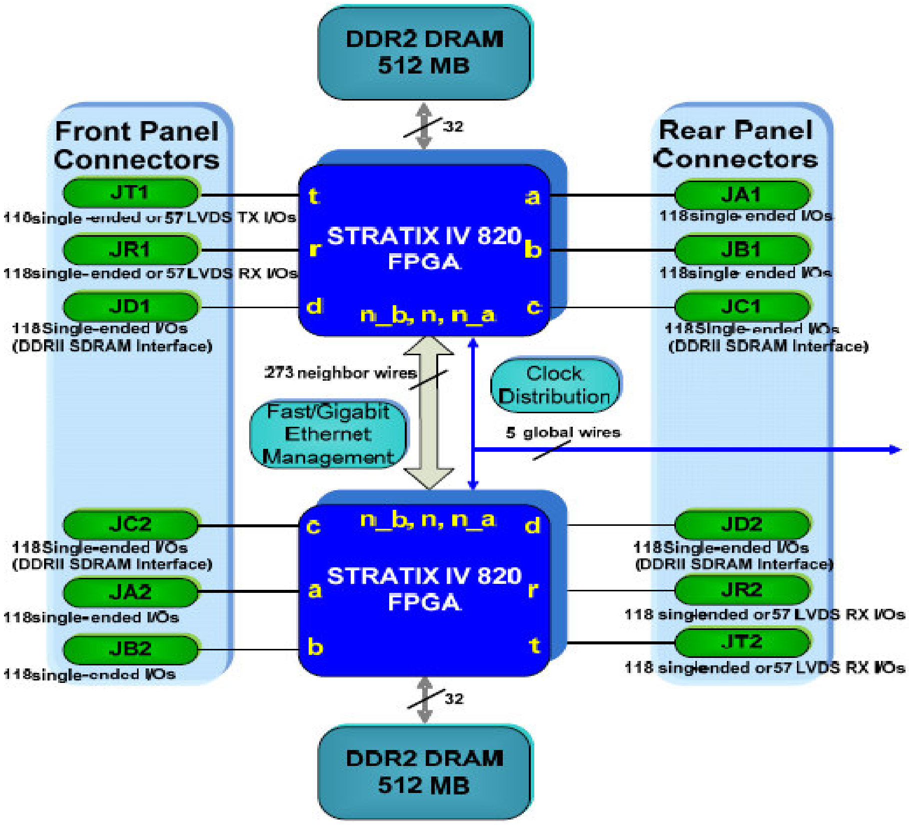
Designed for maximum performance with flexible, high density interconnect

The PROC_SoC has a unique, flexible interconnect topology that allows any FPGA device to directly connect with large numbers of pins to any other programmable device in the entire system. Users match system interconnects to the topology of the design being verified. There are over 950 pins per FPGA available to connect to (1) FPGAs on the same reconfigurable board, (2) FPGAs on other boards in the same PROC_SoC module, (3) FPGAs on any other PROC_SoC module in multiple module PROC_SoC systems, or (4) user's IOs

The system is architected and designed to operate at system clock speeds up to 300MHz. Test suites and real-time operation with embedded and application software will experience the shortest possible verification time and the most effective system integration before silicon for users.

Unique, scalable hardware system is designed for 6 to 120 million ASIC gates

Two scalable, multiple board, card cage-based configurations are available. The PROC_SoC 10-4S module holds up to ten PROC12M, dual-FPGA, 12 million gate boards. The smaller PROC_SoC 3-4S holds up to three PROC12M boards. Capacities are 120 million and 36 million ASIC gates respectively. Each PROC12M board has two, interconnected, high speed Altera Stratix EP4S820 FPGAs and 1024 MB of onboard DRAM, or 10.24 GB for each full PROC_SoC 10-4S module, and 3.076 GB for the PROC_SoC 3-4S. Each PROC12M has over 1400 FPGA IO's are brought to 118 pin edge connectors for user allocated FPGA-to-FPGA interconnection


DDR2 DRAM 512 MB
32
Front Panel Connectors
JT1
118single-ended or 57 LVDS TX I/Os
JR1
118single-ended or 57 LVDS RX I/Os
JD1
118Single-ended I/Os (DDRII SDRAM Interface)
STRATIX IV 820 FPGA
t
r
d
a
b
c
n_b, n, n_a
Rear Panel Connectors
JA1
118single ended I/Os
JB1
118single ended I/Os
JC1
118Single-ended I/Os (DDRII SDRAM Interface)
273 neighbor wires
Clock Distribution
Fast/Gigabit Ethernet Management
5 global wires
JC2
118Single-ended I/Os (DDRII SDRAM Interface)
JA2
118single-ended I/Os
JB2
118single-ended I/Os
STRATIX IV 820 FPGA
c
a
b
d
r
t
n_b, n, n_a
JD2
118Single-ended I/Os (DDRII SDRAM Interface)
JR2
118 singlended or57 LVDS RX I/Os
JT2
118 singlended or57 LVDS RX I/Os
32
DDR2 DRAM 512 MB

Fast, efficient implementation shortens time to debug

The PROC_SoC system includes a comprehensive suite of best in breed software tools for implementing and debugging designs. ***GiDEL's PROCWizard software manages the data and integrates the files generated by best of breed tools for partitioning, design mapping, synthesis, place and route, and debug trigger logic and data capture***. For each user's development environment, PROCWizard will generate a dedicated driver with optimized performance. This enables fast setup and running of comprehensive test benches from a host across a network to the verification system, and co-development with software development tools running on a host

PROC_SoC Finds and Helps Resolve More Bugs Faster

With the PROC_SoC System, tests will run the fastest of all comparable systems, and those hard to reach bugs are found quicker. There are various methods of capturing data and debugging designs to meet the needs of teams at different phases of their projects. Debugging can use both distributed memories within the FPGAs and on-board memories to capture signal data. The PROCWizard debug GUI enables direct access to the design IOs and running of tests. Scripts are automatically generated of test processes for replay. The configurable multi-port, on-board memories can be easily set up to capture data from thousands of probe points during testing with virtually unlimited depth. Also, with the supplied Signal Tap II software, or with debugging tool Total History.

Sharable, scalable capacity

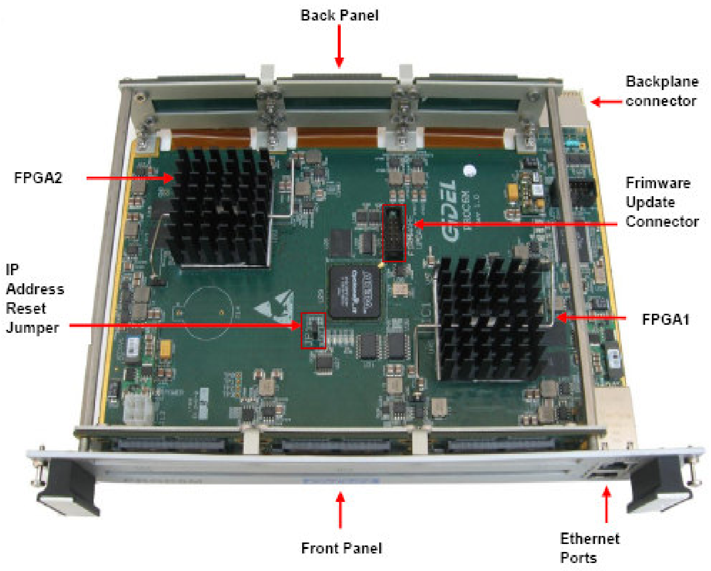
Teams only purchase the capacity they require, and add more capacity as needed. The PROC12M boards fit into a PROC_SoC module card cages within compact cabinets. Multiple PROC_SoC modules can be used for extremely large designs. Further, multiple users can independently access different reconfigurable boards in the same PROC_SoC module for independent designs and block-level regression tests. **Fast/Gigabit networking interfaces to the PROC_SoC modules** dynamically allow the system to be directly linked to various computers for running the test benches and for very fast device programming. The system is complemented by a suite of application specific PROC system daughter boards for direct system interfaces like DDR 2 interfaces, HD-SDI, DVI, PHY/Ethernet, etc. Specifications are provided for design teams to also build their own proprietary daughter boards.

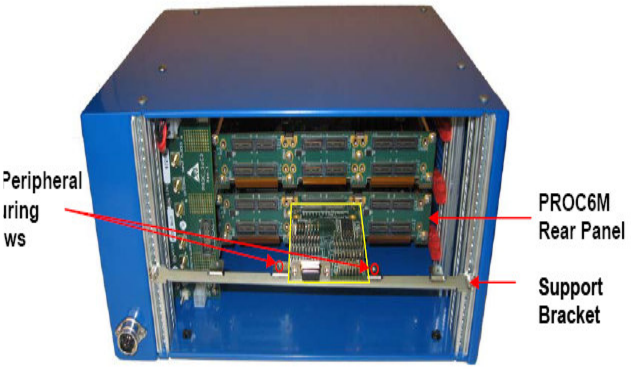
System Integration before Silicon

To enable software development early in the design process, the reasonable pricing of the fully configured systems makes them ideal for supplying multiple test-beds for software development teams to begin verification of software prior to silicon availability. As software is developed, it can be exercised running at hardware speeds savings months of development time. In many cases that by itself will put the SoC into production earlier.

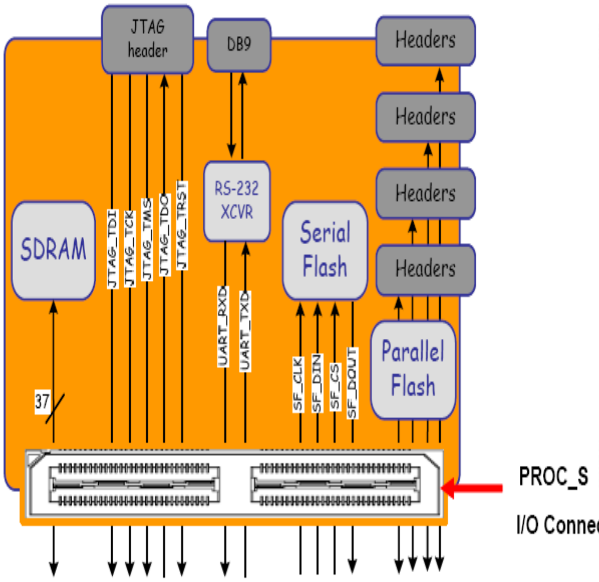
Prototyping Setup

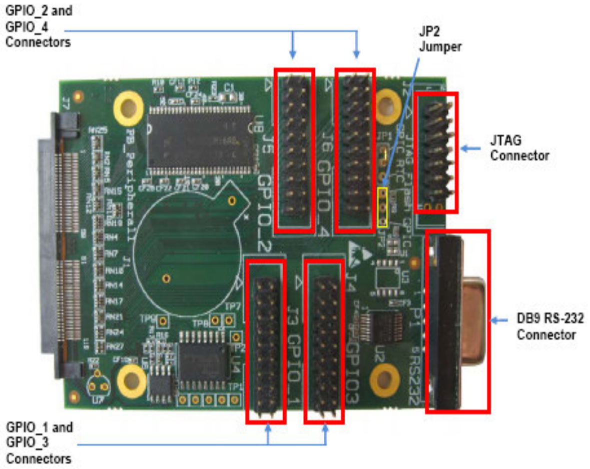
The PROC_SoC 3™ SoC prototyping system is tremendously flexible allowing optimal resource customization to meet target prototyping demands.



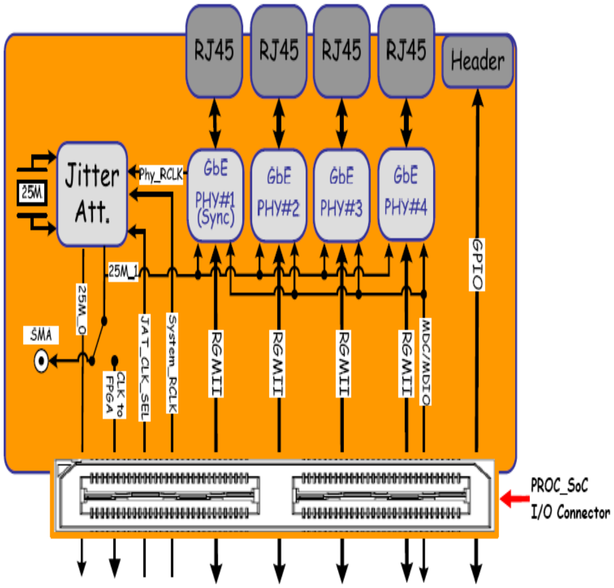


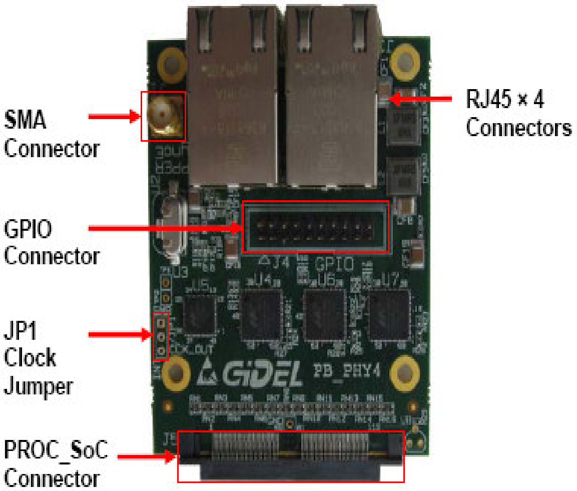
PB_Peripheral1 daughterboard enables the PROC_SoC system to connect to SDRAM, Serial Flash and Parallel Flash memories, and to logic analyzer general purpose I/Os (GPIOs)





The PB_PHY4 is comprised of four RJ45 connectors connected to Gigabit Ethernet ports, a 20-pin GPIO header connector, an SMA coax connector, and a PROC_SoC I/O connector as illustrated in the following system diagram





Partitioning and Implementation

The capacity of the FPGAs has grown much faster than their pin count. So there simply aren't enough physical pins to interconnect blocks that end up on different FPGAs. So, GiDEL's integrated environment offers the option to use Auspy's ACE Compiler. ACE maps designs in RTL or gate-level onto GiDEL's PROCSoC prototyping systems. In addition to FPGA's, connectors, cables, bus switches, daughter cards, clock distribution scheme, power regions, and LVDS interconnects on the PROCSoC target prototyping hardware. ACE takes designs in RTL or gate-level together with the target performance and the board description of the PROCSoC system in Verilog all the way through synthesis, partition, board routing and FPGA synthesis, P&R to produce the downloadable FPGA bit-streams and the on-board cable setups. The flow can be completely automatic, or semi-automatic if the user decides to work on any portion of the mapping by him. Every step can be verified with the test bench in order to isolate and eliminate any possible mistakes that are introduced in the specified step, and therefore, smoothly bring up the hardware. The working compile can be reproduced for the future design revisions through scripts.

Fast design iterations

Implementation is a critical phase in the FPGA prototyping flow. The partitioned design may undergo much iteration as bugs are discovered and fixed, or design blocks are tweaked and re-tweaked for higher performance.

It is very important to keep this iteration loop as short as possible. However, the combination of leading-edge ASIC designs in the multi-million system gate range, and stretch performance goals to model real-world operation, can lead to lengthy synthesis and place-and-route passes. The great advantage that FPGAs offer for debugging and design exploration begins to diminish when using traditional FPGA flows and large design sizes. The answer is to use incremental implementation methods.

In last 10 years, total LEs have grown 35X, memory bits >100X, but computing power only 10X. Altera is addressing compile time on 3 key fronts:

1. **Faster raw compile speed**
   –Continuous improvement in core place-and-route algorithms
   –In 40 nm, Altera leads nearest competitor in 3 key compilation areas: compile time, resulting fMAX, peak memory usage

2. **Multi-core computing**
   –Today, multi-CPU support yields up to 25% faster vs. single CPU
   –Further parallelization efforts will increase this over time

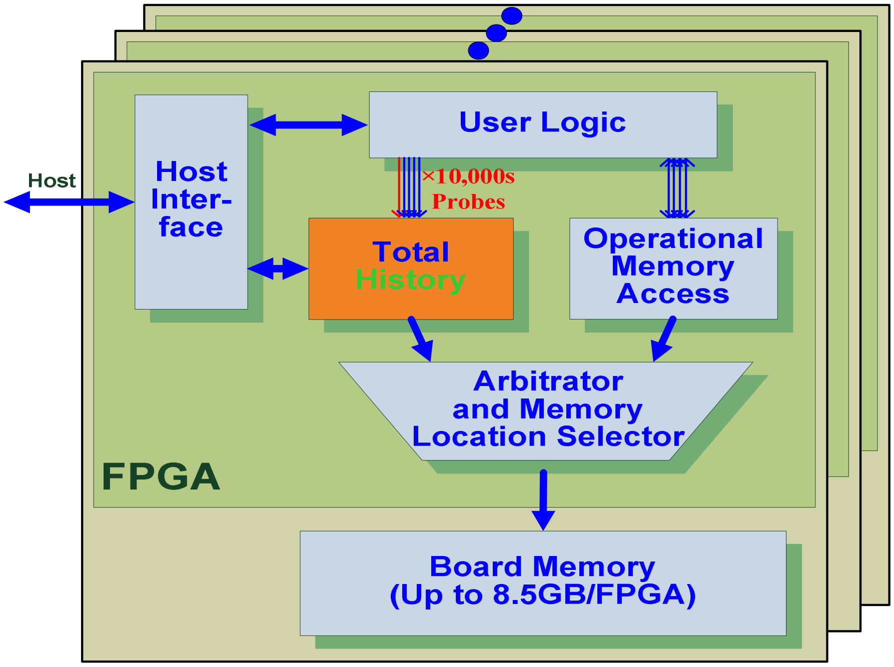
3. **Incremental compile support**
   –Can save 70% in compilation time for a given project, across alliterations

Design Debugging

This is typically where the majority of your time is spent on a prototyping project. The ability to debug any portion of the design quickly and accurately is critical to project success. Let us consider two methods for embedding Virtual Logic Analyzers into the design so as to allow logic and embedded software designers to debug their FPGAs in real time. The two methods are Signal Tap II from Altera and Total History debugging tool (GiDEL)

The main verification tools used today are software RTL simulators, hardware emulators, and FPGA prototyping. Emulators' performances are shadowed by their expensive price, while simulators low price comes at the expense of serious speed degradation. FPGA prototyping provides an integrative solution combining high performance at an affordable price. Prototyping enables real-time performance before tape out, thus verifying the design in its actual target environment and allowing for early SW development and system verification.

FPGA prototyping, however, has suffered from lack of vital visibility to the design's internal states. Without sufficient visibility, verification is very limited and capturing non-deterministic and intermittent bugs is virtually impossible.

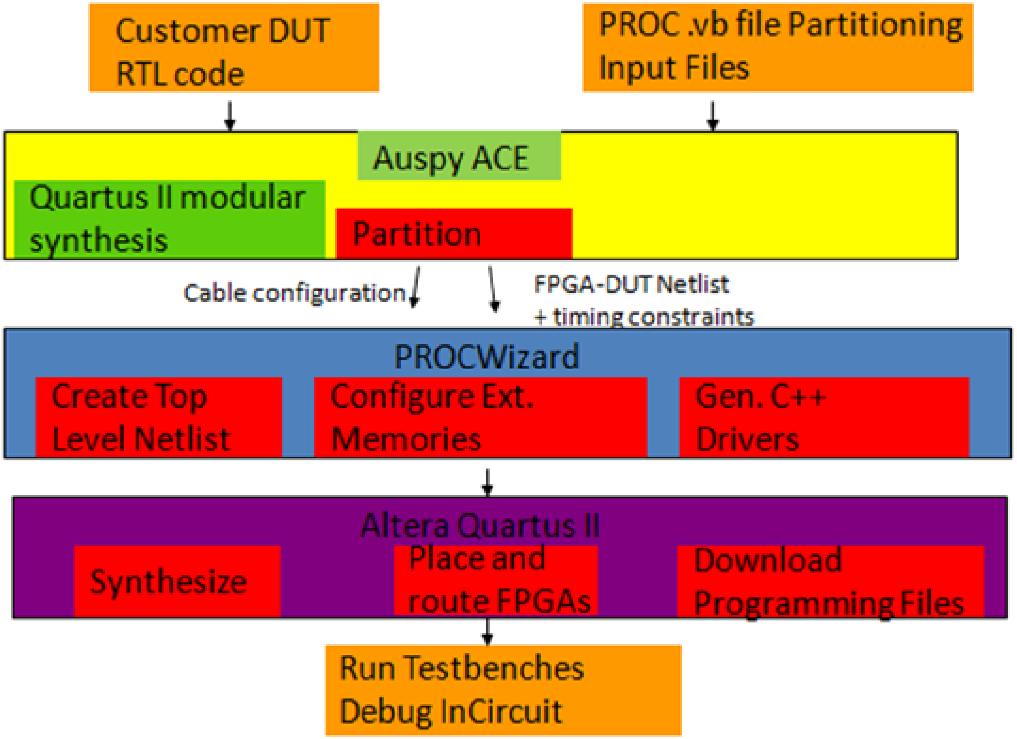

User Logic
Host
Host Inter-face
×10,000s Probes
Total History
Operational Memory Access
Arbitrator and Memory Location Selector
FPGA
Board Memory (Up to 8.5GB/FPGA)

GiDEL's TotalHistory™ IP is an innovative signal tracing tool for FPGA prototyping enabling virtually unlimited signal trace depth, and massive and flexible probing at real system performance. TotalHistory remarkably utilizes the GiDEL FPGA board's unused on-board memory and memory bandwidth, thus needing no additional resources!

GiDEL's novel TotalHistory IP opens the way to unprecedented design visibility. TotalHistory is based on a unique design-embedded IP core. Probes are inserted at any design point of interest to capture signals at full operating speed; signal trace is stored on the on-board memory or on peripheral SODIMMs at practically unlimited depth (up to 8.5 GB/FPGA) enabling virtually infinite signal tracing regression to accurately detect, reproduce and isolate system bugs. Real-time signals are channeled to host allowing user application processing to generate complex triggering schemes to detect bugs and to capture vital internal signal states. Once a trigger is issued, virtually infinite signal trace history can be retroactively analyzed by the host application or by a simulator via the PCI/e bridge or via Gigabit Ethernet (in the case of PROC_SoC™ system). TotalHistory can support as much as 100,000 fully configurable probes per FPGA permitting comprehensive signal visibility.

Integrated Development Environment (IDE)

PROCWizard – GiDEL's Integrated Development Environment (IDE) enables ASIC/SoC verification engineers to create their system architecture at the FPGA level. By providing the entire standard infrastructure that supports FPGA development, GiDEL's PROCWizard lets you focus on developing your unique processing components rather than on the infrastructure around it. While FPGAs provide significant performance benefits, the FPGA development process can be both time-consuming and difficult. PROCWizard s/w addresses these limitations by providing infrastructure that supports FPGA development at a higher abstraction level.

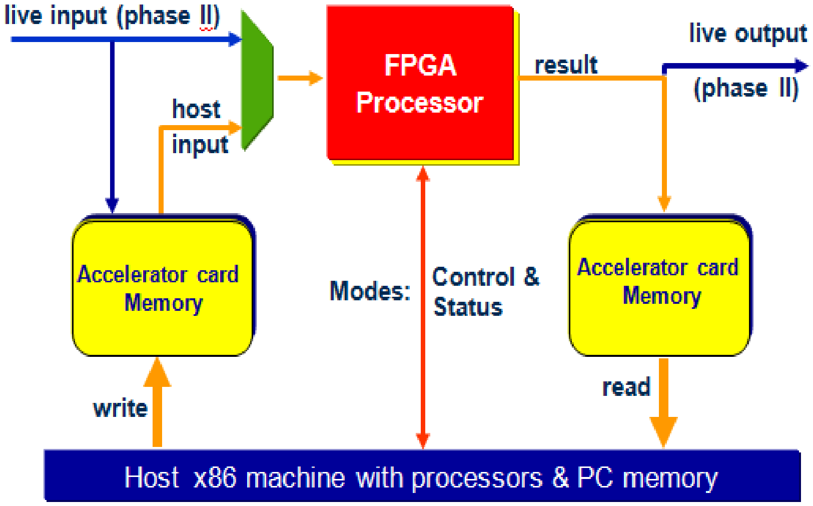


The PROCWizard automatically connects between the SW and the HDL applications running on the PROC Boards. As a result, HW & SW engineers are able to interact and work much closer together. Using the PROCWizard tool with the PROC Boards constitutes a real re-configurable computing environment. The PROCWizard generates an Application driver (a C++ class) for each application / configuration. The PROC Boards application / configuration is changed simply by closing the previous Application driver class and initiating a new Application driver class. For more complex designs, it is possible to reconfigure just part of the devices while the other ones are still working.

These tools shorten our customers' learning curve while increasing their productivity, allowing them to reduce development costs and shorten their time to market.

Need for Real Time Processing

A system level block diagram shown in Fig below, illustrates of how live data can be streamed in/out (through a high speed GigE interface) on ASIC Prototyping system. The data streamed in could either be stored on-board memories or processed directly by the FPGA processor. The processed data could either be stored back on-board memories or sent out to the external world. Data stored on FPGA accelerated system can be sent in a seamless manner to the Host PC memory for further processing or analysis



Memory accesses from/to FPGA

Life Cycle & Quality Management

We want to be sure that our customers are confident in our products and in knowing that we will support them throughout their product lifecycle – from initial design to final production, and into the future. Cutting-edge products backed by a full software suite and quality technical support enable our customers to go to market quickly. Our quality procedures, extended warranties, and technology escrow agreements ensure product quality, reliability, and availability.

References and Acknowledgements

1. For more information on GiDEL FPGA accelerator cards and tools, please visit www.gidel.com

2. For more information on Altera's FPGAs and tools, please visit www.altera.com

3. Versatile FPGA-Based Functional Validation Framework for Networks-on-Chip Interconnections Designs- J.B. Perez Ramas, D. Atienza, M. Pe´on, I. Mag´an, J.M. Mend´ıas, R. Hermida

4. For more information on ACE compiler, please visit www.auspy.com

5. For more information on Synplify Pro synthesis, please refer to www.synopsys.com

6. For more information on Precision RTL synthesis, please refer to www.mentor.com