ETLogic™

OVERVIEW

ETLogic is a state-of-the-art solution to test the digital logic component of integrated circuits. It includes unique features targeted at nanometer SOC designs that reduce test costs and shorten time-to-market while improving quality by reducing test escapes that result in costly field returns. ETLogic uses LogicVision’s patent pending Burst-Mode™ scan architecture and timing to apply an at-speed structural test under functional mode signal integrity conditions. This provides both very high transition fault coverage as well as signal integrity screening through run-time control of at-speed burst cycles. ETLogic’s embedded test IP circuitry can combine the application of pseudo-random and compressed deterministic patterns to achieve unparalleled defect coverage, measured with both stuck-at and transition N-detect coverage metrics. A hierarchical architecture provides both high scalability and full core reuse leading to significant integration efficiencies and time-to-market savings. A fully-automated analysis, generation and insertion flow at either the RTL or gate level ensures low impact to the design schedule. Full and tight integration to all major third-party physical design flows ensures no impact to design performance.

BENEFITS

- Reduced Test Costs:
  › Short test times
  › Minimal tester hardware requirements
- Reduced Field Returns:
  › High transition fault coverage
  › Signal integrity screening
  › High coverage of un-modeled defects
- Shortened Time-To-Market:
  › Quick DFT integration
  › Test pattern debug time reduced or eliminated
  › Fully re-usable embedded test inserted cores

CAPABILITIES

- Comprehensive RTL or gate level automation flow for fast test integration
- Patented BurstMode test timing architecture for true at-speed test application and power control
- High bandwidth pseudorandom test pattern application for high N-detect (defect coverage)
- IEEE 1500 compliant distributed test access architecture and patented core level Shared Isolation for hierarchical test integration
- On-chip run-time programmable masking for X-state handling
- ATPG compression providing over 10x test time and 100x test pattern volume reduction

Figure 1. Hierarchical ETLogic Infrastructure
ETLogic™

SOLUTION DESCRIPTION

ETLogic is optimized for at-speed test and test power management, and is designed to apply a highly diagnosable structural test under conditions that reflect the functional mode of operation. Its multi-mode architecture shown in Figure 1 has the ability to apply any combination of pseudo-random, deterministic or compressed deterministic patterns, with masking support to handle unexpected unknowns.

Self-Test and Compression

In its main mode of operation, ETLogic applies a self-test using a Pseudo-Random Pattern Generator (PRPG) to drive the scan chains and a Multiple-Input Signature Register (MISR) to compress the scan chain output values into a signature. A key advantage of this fully embedded approach is that a very large number of random patterns can be applied in a limited amount of test time. Not only does this provide for high stuck-at and transition fault coverages, but it also results in very high N-detect counts. The N-detect count measures the number of times each fault in a circuit is detected by a different test pattern. In basic terms, the more times each fault is detected, the more probable it is that other untargeted defect mechanisms are covered as well. Industrial results show a strong correlation between N-detect counts and defect coverage.

The self-test mode of ETLogic can be used as a stand-alone test strategy or in conjunction with the ATPG compression mode, in which compressed patterns (or seeds) are shifted at low speed from the tester to a shadow register in the Test Access Port (TAP) or Wrapper TAP (WTAP) of an embedded block (or core). While each seed is being shifted in, the current test pattern is decompressed by the PRPG and loaded into the scan chains at a frequency, which is runtime programmable, often at a speed higher than the tester speed. Both modes use the same embedded architecture, requiring no additional design effort to take advantage of the unique benefits each of them offer.

At-Speed Test under Functional Conditions

The traditional approach of testing for performance-related defects with ATPG-based solutions has been to generate patterns that target transition delay faults. These patterns are applied using two at-speed functional clock cycles to create a “launch” and “capture” sequence. This approach is often referred to as “broadside” or “double-capture” timing. This technique, however, often lacks accuracy, resulting in test escapes or yield loss. In particular it suffers from what is referred to as “clock stretching.” This phenomenon is caused by the instantaneous drain on power rails during the launch and capture cycles that results in an increase of the clock period, an overly optimistic performance rating of the device, and reduced delay fault detection.

Figure 2. BurstMode Timing
ETLogic leverages an innovative BurstMode scan infrastructure to achieve accurate at-speed test under conditions that reflect the functional mode of operation. During the burst phase (see figure 2), all functional clocks are enabled to produce a burst of clock cycles. The burst is long enough to make sure that the supply has time to stabilize before the launch and capture cycles. For each clock domain, the clock burst is configurable at runtime to mimic the functional mode of operation from a timing and power point of view. This is essential to catch subtle problems related to crosstalk or IR drop, for example. The alignment of synchronous clock domains is preserved.

In addition, to achieve the quality and diagnosability levels needed in nanometer designs, ETLogic uses a launch-on-shift (or skewed-load) approach which has been shown to achieve a 5 to 7 % higher transition fault coverage than when the launch-on-capture (or double-capture) approach is used. The scan enable signal is pipelined locally to each domain in order not to impact timing closure.

BurstMode Timing is a proven technology that has been in production use at leading semiconductor companies.

Hierarchical Scan Test

ETLogic supports a hierarchical architecture (see figure 1) to scale with design size, speed and power. A key component of this architecture is the ability to efficiently isolate each core during test application.

WTAP Architecture and Re-usable Tests

LogicVision’s Wrapper Test Access Port architecture meets the requirements for the IEEE 1500 standard and serves as a hierarchical TAP architecture for a logic block or core. The advantages of this approach are highly reduced global test signal routing, incremental assembly and verification, and containment of timing-critical signals within a hierarchical block or core. In addition to enabling hierarchical methods, ETLogic with its WTAP capabilities allows the creation of “BISTed” cores that are used on any design as fully-testable cores.

The core level diagram in Figure 3 illustrates LogicVision’s patented core isolation technique that uses a combination of existing functional flops (Shared Isolation flops) and some additional flops (Dedicated Isolation flops) to separate the design into independent core components, with minimal area overhead and no impact on performance. Existing functional flops at or near the periphery of the core are used whenever possible to serve as isolation points. Control logic is added to ensure that these flops do not capture data from outside the core during scan testing. Additional flops are sometimes needed to isolate core pins that are not in close proximity to a functional flop. The identification of Shared Isolation flop candidates as well as the insertion of all necessary isolation logic is performed automatically.

A hierarchical test approach is also crucial in managing low power designs. Average power consumption during scan testing tends to be much higher than during functional operation. A key reason for this is that the typical large amount of clock gating used to conserve power must be disabled for the scan operation to work. In order to remain within an overall power budget, scan-based testing must be applied sequentially to each individual core or subset of cores.

Figure 3. Core Isolation Support
Integrated Automation flow

The hierarchical ETLogic infrastructure is added to a design using LogicVision’s advanced LV2005™ automation flow (see figure 4). This fully hierarchical flow ensures limited impact to the design schedule and quick turn-around time. The flow consists of five major steps. The first three steps can be executed on either RTL or gate level netlists. The last two steps are executed post synthesis.

ETChecker is first run to ensure that the RTL meets all LogicVision DFT rules, and then to extract necessary design information for the next steps. In the second step, ETPlanner determines the required embedded test resources using trade-offs based on such information as clock domains, core boundaries, test time and area overhead constraints. Next, ETAssemble generates and inserts all of the necessary embedded test resources and hierarchical test access infrastructure into each of the cores. ETAssemble also generates all necessary support files, such as SDC scripts, to drive the synthesis process. After synthesis, ETScan inserts scan chains and test points if necessary. This step is tightly integrated to all major 3rd party physical design flows and results in no impact on design performance. In particular, ETScan generates a ScanDEF file, which provides the information needed by the physical optimization tool to reorder the inserted scan chains without effecting the BIST operation. After physical optimization and layout, ETSignoff auto-generates the final initialization vectors for manufacturing test and verifies these vectors through simulation.

Figure 4. Automated DFT Integration Flow