

Driving 3D Chip and Circuit Board Test Into High Gear

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Emerging Standards and 3D Chip Test

Taken independently, the pending ratification of one IEEE standard and the recent ratification of another will each have significant effects on characterizing, debugging and testing multiple-die 3D chips. But taken together, the two standards will profoundly accelerate the quest for higher 3D chip yields, lower test development costs over the entire product life cycle and quicken the time-to-market for system manufacturers.

The two standards are the recently ratified IEEE 1149.7 Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture and the preliminary IEEE P1687 Internal JTAG (IJTAG) standard for accessing on-chip embedded instrumentation. Both are expected to be ratified soon (1149.7 was ratified at the end of 2009 and P1687 is on target for ratification during the latter half of 2010). ASSET InterTech and its ScanWorks platform for embedded instrumentation are well positioned to take advantage of these standards to their fullest. ScanWorks is an open platform that can quickly accommodate new capabilities and ASSET experts are in leadership positions on the working groups that have been developing both

standards. Al Crouch, ASSET's chief technologist - core instrumentation, is co-chairman of the P1687 working group, and Adam Ley, chief technologist - boundary scan, has served as the primary author and source of the test content in the 1149.7 standard.

Extending Moore's Law

Certain experts in the industry have asserted that 3D chip packages with multiple silicon die will be the most effective way for the industry to continue extending Moore's Law, which predicts a doubling of circuit density every 18 months to two years. The physics of chip fabrication process geometries below 90nm are daunting. Some system manufacturers are finding it easier to stay with multiple die fabricated at larger process geometries and placed in a 3D package than to move to chips processed at smaller submicron geometries. This has accentuated the critical nature of standards for characterizing, debugging and testing 3D chips before they are placed on circuit boards, as well as validating, debugging and testing circuit boards after 3D chips have been placed on them. The two emerging standards - 1149.7 and P1687 - address the 3D issues at the bare die, packaged chip and board levels.

Embedded Instrumentation

For several years now, chip manufacturers have embedded test and measurement instrumentation into their devices in order to verify and test these devices from the inside out, instead of relying solely on external equipment such as “big iron” Automatic Test Equipment (ATE) IC testers that test from the outside in. For instance, memory and logic built-in self-test (BIST) engines,

tact. One solution is to eliminate physical contact from the test process by embedding instrumentation into chips and employing it in chip and board test applications.

Another impetus behind the trend is the goal to provide more information rather than purely raw data. Contemporary time-to-market pressures require that debug, diagnosis and failure analysis be conducted more intelligently. Ideally, test results

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and internal scan and scan-compression have been embedded in chips for some time. A proprietary example of embedded instrumentation is Intel’s Interconnect Built-In Self Test (IBIST) which that company has been embedding into its next-generation chips and chipsets to enable high-speed IO test, characterization and tuning.

One impetus behind this trend has been the increasing inadequacies of external probe-based test equipment, such as oscilloscopes, logic analyzers, in-circuit test (ICT), manufacturing defect analyzers (MDA), flying probe testers and other hardware approaches that rely on making physical contact with pins on chips or test pads on circuit boards. The state of the art in the electronics industry today is such that this physical contact can disrupt and obfuscate characterization, validation and test measurements to the point where real faults or failures cannot be distinguished from those anomalies introduced by the physical con-

or collected data would be localized to a time and place within the chip instead of the mismatch that often takes place on a package pin or the 10,000 cycles of data taken by brute force collection methods at the pins of the package.

Access, Automation and Analysis

As the need for embedded instrumentation has emerged, so too has the need for standard methods for accessing and automating these instruments, and for analyzing their output. As a result, representatives from companies across a wide swath of the electronics industry have come together to develop the 1149.7 and P1687 standards.

Extending Boundary Scan to 3D Chips

At its most basic level, the IEEE 1149.7 standard maintains the access to chips and structures on circuit boards that the origi-

nal boundary-scan standard (IEEE 1149.1) has provided since it was developed in the early 1990s to deal with lack of access due to surface mount technology. (The boundary scan standard is also referred to as JTAG after the Joint Test Action Group that initiated development of the standard.) Boundary-scan access has been deployed in various applications, including circuit board test, the programming of chips in-system and others.

The 1149.7 working group has gone to great pains to ensure that this new standard is completely compatible with the original 1149.1 boundary-scan standard. As the name of the new standard implies, the intent of the working group was to devel-

(TSV), give engineers significantly enhanced capabilities for testing embedded cores or 3D chips individually and after they have been soldered onto a circuit board.

Interfacing to Embedded Instrumentation

The first-generation P1687 IJTAG standard uses 1149.1 boundary scan for physical access to embedded instrumentation inside chips. Since embedded instrument IP (intellectual property) can come from a number of sources, such as chip suppliers, third-party providers, EDA tools or in-house design groups, P1687 is intended as a standard way of connecting, analyzing,

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op a chip-level test access port (TAP) and associated architecture that would offer reduced pin-count from 1149.1 (if needed) and enhanced functionality. Instead of the four-wire 1149.1 interface with an optional fifth wire, 1149.7's TAP offers a range of solutions that include a two-signal solution, although an 1149.7 implementation may include all four (or five) signals.

In addition, the 1149.7 standard includes several architectural enhancements. For instance, support of multiple on-chip 1149.1 TAP controllers is possible under the 1149.7 standard (solving a problem that has grown lately as the 1149.1 TAP is used more and more to access on-chip embedded instrumentation). This and other features of the 1149.7 standard, such as its reduced pin count, a new glue-less star topology and compatibility with through-silicon vias

describing and using embedded instrumentation no matter where the instrument has come from.

P1687 IJTAG enables a number of functions that will improve the testability of a single chip or multiple die in a 3D chip. The three primary functions are: 1) documentation of embedded instrumentation; 2) reuse of embedded instrument vectors; and 3) test scheduling. For example, IJTAG could be used to automate and schedule the parallel operation of multiple embedded instruments such as multiple memory BIST engines. IJTAG would allow flexible access to only those engines that are required for a certain test process. Or, IJTAG could launch an embedded logic BIST engine for chip test that might be parallel with a voltage monitor intended for yield analysis. The resulting simultan-

eous operation of these two embedded instruments could determine whether failures identified at the ATE or board levels correlated with voltage starvation.

Putting the Two Together

Deployed together in the same chip, 3D multiple-die device or circuit board, 1149.7 and P1687 form a potent solution for performing chip-level characterization, debug and test as well as board- and system-level validation, debug and test. In fact, the portability of this test methodology from the chip level all the way to the system

level delivers huge benefits to manufacturers. Until now, during each phase of chip and system development, characterization, validation, debug and test routines were developed independently of each other. So, chip-level characterization and test routines would not migrate with the devices when they were deployed onto circuit boards and in systems. New test routines would be redeveloped for circuit boards and again for systems. In effect, the same work would be performed all over again at each level of integration. Embedded instrumentation and the inter-

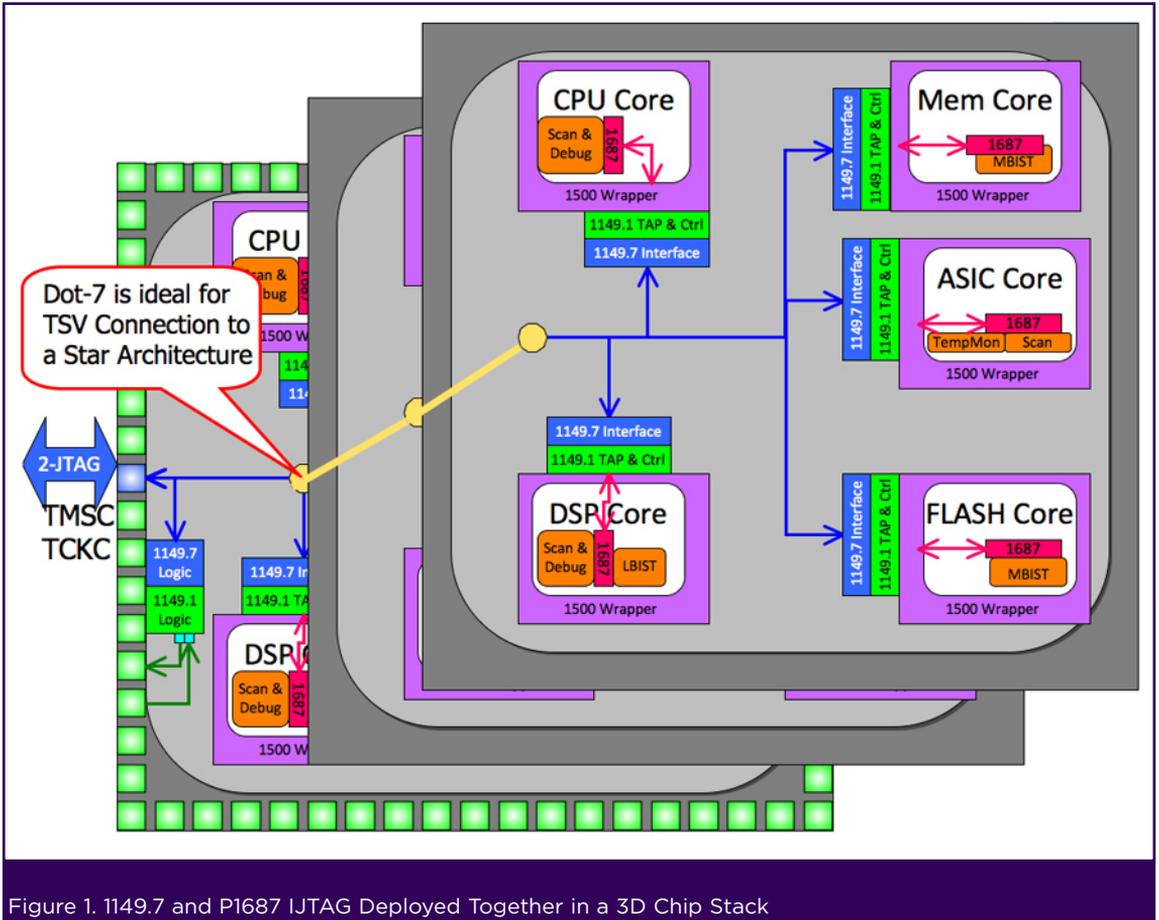


Figure 1. 1149.7 and P1687 JTAG Deployed Together in a 3D Chip Stack

play of 1149.7 and P1687 have the potential to change this so that test routines developed for instruments, cores and chips can migrate with those devices and be reused throughout the entire life cycle of systems. For example, P1687's instrument connectivity language (ICL) and procedural description language (PDL) together function much like the boundary scan description language (BSDL) of the 1149.1 standard when it is used in conjunction with serial vector format (SVF). However, PDL allows instrument-level vectors to migrate and be reused again and again. In addition, PDL allows some flow control (if-then, for-next, etc.), whereas SVF does not. Better, more thorough tests would result, as well as huge

cost savings from significantly reduced test development efforts.

Figure 1 shows how the 1149.7 and P1687 standards could be implemented in a 3D chip package, but the same principles would apply to single-die chips and board-level deployments.

The multiple die stacked on top of one another in this illustration are connected vertically with TSV (represented by the yellow dot in the drawing) and a two-wire implementation of 1149.7. A broadcast star architecture on each die would connect each of the several cores on that die. The cores could each support an 1149.1 TAP, or a single 1149.1 TAP might be deployed at the die level and provide access to all core wrappers and

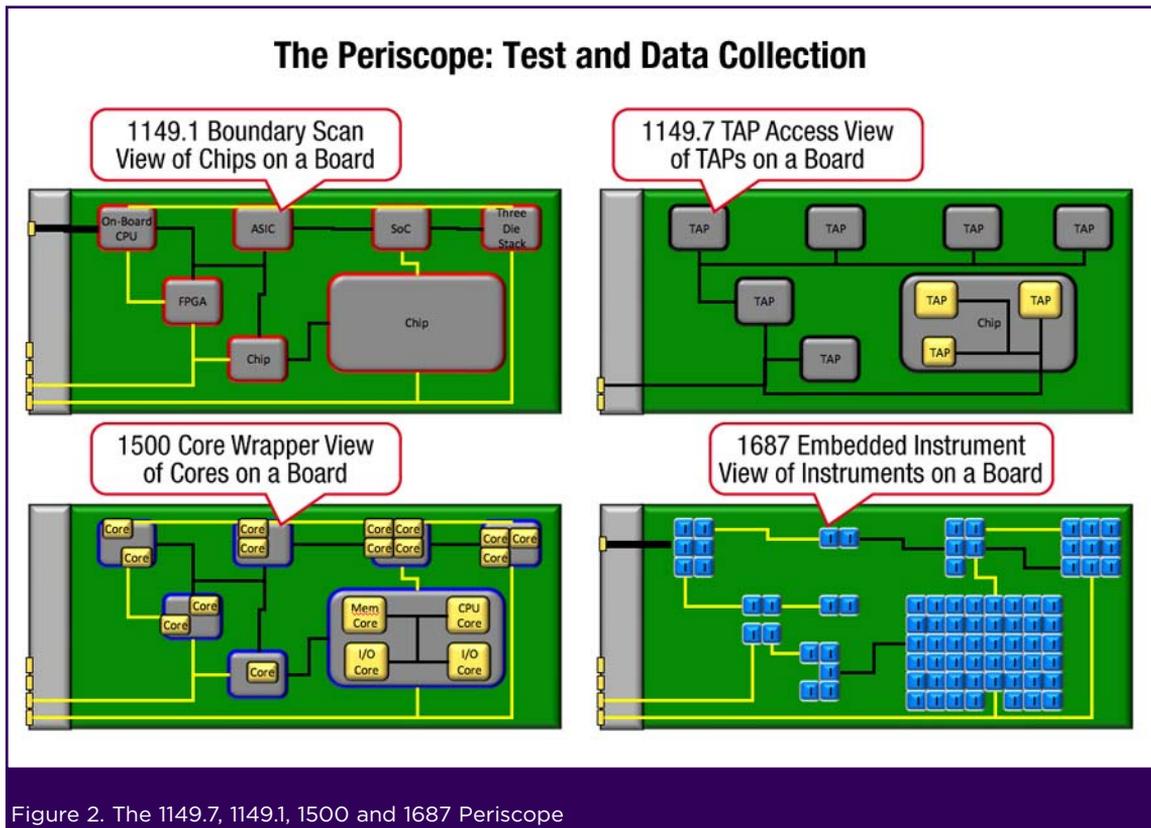


Figure 2. The 1149.7, 1149.1, 1500 and 1687 Periscope

embedded instruments on that die. A P1687 IJTAG interface on the embedded instruments would be used for standardized access and to coordinate all of their operations through the various 1149.1 TAPs.

When placed on a PCB with other chips and possibly other multiple-die stacked packages, the architecture continues to scale. Multiple chips can be connected in a daisy chain or by continuing the broadcast-star architecture from the multiple-die stacked package. From the standpoint of the test software, there could be multiple P1687 instruments each with its own address; or a collection of IP Core 1500 test wrappers. 1149.7 test software would see the situation as a collection of TAPs on the board, much like 1149.1 boundary scan views multiple chips with boundary scan at the board level. Tests at each of these levels could be applied and intermixed and intermingled if necessary. (See Figure 2 for an illustration of how the various standards might be deployed on a circuit board.)

By standardizing much of this scenario, third-party tools like ASSET's ScanWorks platform for embedded instrumentation can be deployed as a test executive to apply all sorts of test routines for chips, circuit boards and systems. And, since ScanWorks is an open platform, tools or processes from other third parties can plug into the platform to extend its capabilities.

The Future of Embedded Instrumentation

Certainly new standards require time to be deployed and promulgated throughout the industry, but history has shown that open standards can provide the basis for markets to develop where technology suppliers innovate and compete with one another to provide the most cost-effective solutions possible. Certainly this is what will transpire in the marketplace for embedded instrumentation tools for single-die chips, complex SoCs, multiple-die 3D chips, circuit boards and systems.

About the Author

Al Crouch

Al Crouch has been in semiconductor DFT and test for over 20 years and is currently the chief technologist and director of IJTAG R&D for Core Instruments at ASSET InterTech in Richardson, Texas. His current responsibilities are driving product development for accessing and operating embedded instruments, developing embedded instruments for IC DfX and driving data collection technology for correlation of ICs on boards and on IC ATE. He is the author of the best-selling "Design for Test for Digital IC's & Embedded Core Systems," and an inventor on more than 15 issued U.S. patents in the field of test. ■