

SCANWORKS® PCI-100 BOUNDARY-SCAN CONTROLLER

PRODUCT OVERVIEW

The PCI-100 IEEE 1149.1 boundary-scan controller provides a sustained data throughput at high TCK frequencies allowing very fast test and in-system programming application times. The PCI-100 supports one Test Access Port (TAP) interface to the board and two TAP control modes. By supporting two different TAP control modes, the PCI-100 enables support of non-compliant, boundary-scan devices and special board test operations. It uses the industry-proven Texas Instruments SN74LVLT8980 embedded Test Bus Controller (eTBC) for dependable scan operations. The PCI-100 supports a controller-to-board distance of 4 feet without the use of the optional pod. The pod extends that distance to 9 feet. Custom-built cables can extend the maximum distance to over 20 feet using lower TCK frequencies. The optional pod also expands the supported voltages from 3.3V (5V tolerant) to a

range of 1.8V to 5.0V. The PCI-100 also supports 16 individually controllable discrete I/O signals for controlling and monitoring non-boundary-scan signals.

PCI-100 PRODUCT

The base PCI-100 product includes:

- One controller card
- One PCI card-to-board TAP cable (4 feet)
- One PCI card-to-board TAP cable (8 inches)

An optional discrete I/O cable (connects PCI-100 card-to-board being tested) is available (no connector at board end, 10 feet). The optional pod adds:

- One pod
- One PCI card-to-pod cable (5 feet)

The card-to-board cable provided with the controller card is compatible with the pod-to-board connector, eliminating the need for another cable.

PCI-100 PROGRAMMABLE CLOCK

The TCK signal provided by the PCI-100 controller card is programmable in eight increments from 130 kHz to 16.6 MHz. This allows you to select the maximum TCK frequency your board will support, enabling the fastest test and programming times. The TCK frequency is controllable from the ASSET hardware setup menu or from the FREQUENCY statements in SVF and STAPL files.



PCI-100 FLEXIBLE TAP SUPPORT

The PCI-100 supports two modes of controlling the TAP signals:

- Gated TCK (default mode)
- Free running TCK

In the gated TCK mode, the TAP controller will not enter the PAUSE-IR or PAUSE-DR state during a data shift operation. If the data buffer needs to be reloaded, the TCK signal is inhibited until it is again ready for data transfers. This allows support of in-system configuration of FPGAs and some non-compliant devices, as well as support for multi-drop backplanes configured with the Texas Instruments Addressable Scan Port (ASP). The PCI-100 is capable of shifting data at continuous 16.6 Mbits per second without gating the TCK during scan operations.

The free running TCK mode applies a continuous TCK signal to the board, using the PAUSE-IR and PAUSE-DR states to reload shift buffers if necessary. This mode supports designs and devices that require a continuous TCK signal.

PCI-100 DISCRETE IO SIGNALS

The PCI-100 controller card supports 16 non-boundary-scan signals that can control inputs to the board or observe outputs from the board. The state of these signals can be controlled and observed using the ASSET macro language or from ScanWorks™ interactive applications such as the debugger. These signals are all bi-directional and controlled individually. These signals are open-collector outputs with LVTH level (3.3V, 5.0V tolerant) input monitoring. Eight signals are terminated for high drive and eight are terminated for low load characteristics. See the PCI-100 documentation for specifications.

PCI-100 BOARD VOLTAGES

The PCI-100 controller card supports 3.3V (5.0V tolerant) input/output signals. With the provided cables and properly terminated and driven signals, the controller card supports a TCK frequency of 16.6 MHz at a distance of 4 feet to the board or system under test. Lower frequencies have been verified to operate up to eight feet from the controller card.

Support for board voltages from 1.8V to full 5.0V is provided with the optional pod. Support for 1.8V, 2.5V, 3.3V, and 5.0V is either automatically or manually selected. If a reference voltage from the board is provided, the pod automatically selects the proper interface. Alternatively, the interface can be selected with switches provided on the pod. LEDs on the pod indicate the selected voltage. See the PCI-100 documentation for specifications.

PCI-100 DIFFERENTIAL TAP SIGNAL SUPPORT

The PCI-100 controller card provides differential output signals to allow the pod or a test fixture to be located more than 16 feet from the host PC, at the maximum TCK frequency of 16.6 MHz. Differential signal specifications are provided allowing you to design the interface into your test fixture. This eliminates the need for the pod.

PCI-100 TAP MONITOR PORT

The optional pod provides external signals to monitor the current TAP state, the TCK and TMS signals, and the DR and IR shift signals. These signals are especially useful to monitor software control of the TMS signal when verifying a new TAP controller design in a custom device.

PCI-100 PHYSICAL FEATURES

The PCI-100 and pod are built to commercial environmental standards for the U.S. and Europe. The pod is EMI shielded to eliminate noise in a laboratory or manufacturing environment. See the PCI-100 documentation for complete specifications.

FULL LIFE-CYCLE SUPPORT

During the design/debug or the field service stage of your product's life cycle, the PCI-100 controller card provides you with a robust and flexible interface from your host test platform to your board. It is fast enough to provide maximum scan throughput to all but the most highly optimized scan paths, yet inexpensive enough to be used in high volume production. By using the same controller in design/debug test development and manufacturing, you eliminate any question of compatibility. Also, if you have an

In addition, selecting a device or pin allows you to view its properties or display the relevant part of the scan path. The fault coverage is viewed by generating a combined coverage report and clicking on the provided links. A link is provided to display the interconnect fault coverage report which contains links to display all the nets in each of the six coverage classes, from fully covered to no coverage. The combined coverage report includes links to display the opens coverage at the device and pin level. All fully covered devices (all pins covered) and all devices with no coverage can be displayed, as well as any partially covered device with the covered pins highlighted.