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SPRINGSOFT SIMPLIFIES VERIFICATION OF LOW-POWER CHIPS WITH ADVANCED POWER-AWARE DEBUG SOLUTION

*New Verdi Power-aware Debug Module enables visualization of power intent
with RTL and UPF/CPF for automated debug and analysis*

HSINCHU, Taiwan, February 8, 2010 — SpringSoft, Inc. (TAIEX: 2473), a global supplier of specialized IC design software, today introduced a new power-aware debug module for its award-winning [Verdi™ Automated Debug System](#). Power-aware debug accelerates the comprehension of power intent and automates the process of visualizing, tracing and analyzing the source of power-related errors. The module is fully integrated with the hardware description language (HDL) debug capabilities of the Verdi system, the cornerstone of SpringSoft's family of Novas™ Verification Enhancement products that enable engineers to do more verification in less time.

SpringSoft's power-aware debug combines support for the United Power Format (UPF) and Common Power Format (CPF) with design comprehension tools for understanding power intent and automated debug techniques to determine whether unexpected design behavior is caused by functional logic or power-related issues. These capabilities are enabled within the Verdi environment for more efficient understanding and debug of low-power system-on-chip (SoC) designs. An early adopter release of the power-aware debug module is already in use by several top-tier global semiconductor companies.

“While CPF and UPF provide a consistent way of describing power intent from RTL design through verification, there have been no power-aware debug tools available at the RTL abstraction,” said Thomas Li, director of product marketing at SpringSoft. “Verdi bridges this power verification gap by providing a universal platform for integrating

power formats and innovations with HDL debug automation. Now that it's easier to visualize, trace, and analyze complex power behaviors in both RTL and UPF/CPF code, engineers can resolve power issues earlier in the process and save valuable verification cycles."

Power-aware Comprehension & Debug

The Verdi power-aware debug module provides full UPF and CPF source code support with the ability to import and compile data from these power design languages into SpringSoft's design Knowledge Database (KDB). This provides a high-level view of power intent that can be correlated with RTL design data also contained in the KDB to give a complete power-aware picture of the design structure.

An easy-to-use Power Manager browser enables engineers to visualize and annotate power intent in traditional RTL design views (source code, schematic, and waveform). Power-related constraints such as level shifter and switch rules can be easily located for each power domain and correlated to specific RTL design blocks. With the ability to cross probe between power and RTL views, engineers can readily identify the origin of power-related problems.

Leveraging the advanced RTL debug capabilities of the Verdi system, engineers can then track down the root cause of power-related behavior across RTL and power domains. The paths of signals driven by CPF/UPF code are automatically traced throughout different power domains, so debug is directed to the relevant source. Dynamic power modes/states are annotated in both RTL and power views for seamless tracing between RTL and CPF/UPF code during debug. In addition, the current power status of any signal can be quickly checked and traced to its CPF/UPF source.

A detailed technical paper describing power-aware debug requirements and solutions is available on the SpringSoft web site at: www.springsoft.com/whitepapers/power-aware-debug.

Verdi Automated Debug System

The Verdi Automated Debug System is SpringSoft's flagship product for advanced debug. It cuts debug time in half by automating the process of comprehending how complex IC and SoC designs work. The full-featured system automates behavior tracing over time with its unique analysis engines, provides a powerful set of design views to

visualize and help analyze cause-and-effect relationships, and uses patented techniques to reveal the functional operation and interaction between the design, assertions and system testbench.

Pricing & Availability

The Verdi Power-aware Debug Module is immediately available at U.S. list price of \$5,000 for a one-year subscription license. It is fully supported with the latest release of the Verdi Automated Debug System, which is U.S. list priced at \$14,000 for a one-year subscription license.

About SpringSoft

SpringSoft, Inc. is a global supplier of specialized automation technologies that accelerate engineers during the design, verification and debug of complex digital, analog and mixed-signal ICs, ASICs, microprocessors, and SoCs. Its award-winning product portfolio features the Novas Verification Enhancement and Laker Custom IC Design solutions used by more than 400 of today's leading IDM and fabless semiconductor companies, foundries, and electronic systems OEMs. Headquartered in Hsinchu, Taiwan, and San Jose, California, SpringSoft is the largest company in Asia specializing in IC design software and a recognized industry leader in customer service with more than 400 employees located in multiple R&D sites and local support offices around the world. For more information, visit

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