Approaching Board Test Nonintrusively

by Alan Sguigna, ASSET InterTech

It's inevitable. Basic electronic technology evolves. Chips and circuit boards are designed and made differently today than they were 10 years or even five years ago. It stands to reason that the technologies that manufacturers have deployed to test chips and circuit boards would evolve right along with the chips and boards.

In a quiet way, test methods have evolved. But now the test industry is fast approaching a tipping point where the older, intrusive, hardware-based test techniques must be complemented, supplemented, or outright replaced by newer, software-driven, nonintrusive test technologies. What's driving this trend is what has always driven the test industry: test coverage. Without it, test engineers look elsewhere, and that's what they're doing today.

New nonintrusive board test (NBT) techniques are making significant inroads for two reasons:
• Test coverage is eroding because today's evolved technologies can't be tested with the old methods.
• The economics of today's electronics industry demands more cost-effective test methods such as NBT.

Where's the Coverage Going?

Nonintrusive test technologies like boundary scan (JTAG), processor-controlled test (PCT), and certain types of BIST such as Intel's Interconnect Built-In Self-Test (IBIST) have a big advantage over the older, intrusive test technologies, including in-circuit testers (ICT), manufacturing defects analyzers (MDA), flying-probe testers, oscilloscopes, and logic analyzers. The software-driven nonintrusive techniques do not require physical contact with a chip or board the way that probe-based or bed-of-nail intrusive technologies do.

Depending on physical contact with chips and test pads on circuit boards is a severely limiting factor for intrusive test. For example, ICT fixtures rely on making physical contact with test pads on circuit boards (**Figure 1**).

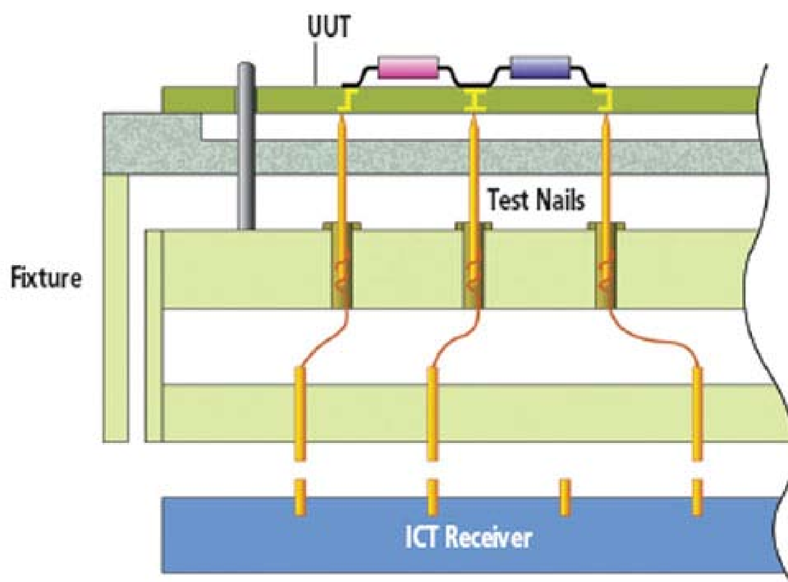

Figure 1. ICT Test Fixture Showing Test Pads

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Unfortunately, fine-pitch devices, high-density interconnects, blind and buried vias, BGAs and other chip-scale packages, heat sinks, conformal coating, AC-coupled high-speed serial I/O buses, and other board design issues now quite commonly prevent physical access for electrical testing. And, without physical contact, there's no test coverage from intrusive test technologies.

In addition to disappearing physical access, contemporary chips and boards are so sensitive that the very act of placing a probe or a nail on them can disrupt the electrical characteristics of the UUT. The disturbances introduced by intrusive test are indistinguishable from faults and failures. And that means that the test coverage once provided by an intrusive test no longer exists.

The new high-speed serial buses and circuit board interconnects like PCI Express (PCIe) 2.0 or 3.0, Fibre Channel, 10-Gb/s Ethernet, InfiniBand, and Intel QuickPath Interconnect (QPI) provide examples of this. If a test pad is designed into a circuit board and located on one of these high-speed interconnects, placing an ICT probe on the test pad introduces capacitive anomalies on the interconnect. The anomalies look just like faults, but they're not. As a result, ICT test coverage on the interconnect disappears.

Nonintrusive Board Test

Because it is software-driven, NBT can efficiently apply multiple test technologies from a single hardware platform to the same UUT. In this way, NBT achieves very high test coverage, recovering all or most of the coverage lost as a result of technology's evolution and, in addition, often testing aspects of the design that intrusive technologies never could.

For example, an NBT test strategy might include boundary scan test, PCT, and a BIST technique such as IBIST. These nonintrusive technologies rely on embedded instrumentation within silicon to deliver test coverage.

Embedded instrumentation can be defined as IP conforming either to an industry standard or a proprietary specification that's embedded within devices and which enables the validation, test, and debug of chips, boards, and systems. The boundary scan infrastructure in chips, which is defined by IEEE 1149.1, can be considered a type of embedded instrumentation.

The development of the boundary scan standard began in the mid-1990s as a reaction to the emergence of fine-pitch pins on chips that could not be probed. In addition, pins were disappearing under the silicon die in chip-scale packaging such as BGAs.

The 1149.1 boundary scan standard defines a four-wire interface called the test access port (TAP). On chips, this is commonly referred to as the JTAG port from the name of the group that first started working on the boundary scan standard: the Joint Test Action Group. Later, the standard was taken up by an official IEEE working group.

Boundary scan has been widely adopted by the industry. In fact, 1149.1 is the basis for several additional standards, including IEEE 1149.6 for high-speed AC-coupled interconnects, a newly enhanced version of 1149.1, and 1149.7.

PCT, another nonintrusive technology, is sometimes referred to as in-target probe (ITP) or processor emulation test. As the name implies, control of the board's processor is temporarily given over to the test platform so the processor can be used to read and write memory and I/O registers in addressable devices on the circuit board. In this way, PCT exercises the functionality of the circuit board and, as a result, detects and diagnoses structural faults. Since it is an at-speed technology, PCT will detect faults that cannot be found by static test technologies like many of the intrusive techniques, including ICT, flying probe, and MDA.

IBIST, a third NBT technique, is a proprietary implementation of BIST that is being embedded into next-generation chips and chip sets by Intel, Avago, and other semiconductor and IP providers. The nonintrusive IBIST functionality can be applied in a number of ways including structural electrical tests in NBT applications. It also can be used in design applications to validate the performance of high-speed serial buses on circuit boards.

IBIST is particularly useful on high-speed serial buses like QPI and PCIe. The sensitive nature of

these buses prevents test pads from being placed on a circuit board to test and validate the performance of the underlying bus. A test pad on one of these high-speed serial interconnects disrupts the signal integrity and functional performance of the circuit board.

Because IBIST is another at-speed nonintrusive technology, it can detect faults and failures that typically would pass low-speed static tests, such as those applied by ICT or boundary scan. These sorts of failures might include microcracks, drift in component capabilities across manufacturing lots, or power supply issues perhaps caused by incorrect or missing capacitors or terminations.

Applying NBT to New Designs

NBT strategies are particularly effective on leading-edge designs. For example, under the codename Nehalem, Intel's next-generation microarchitecture has been spoken of in the industry for quite some time. This technology, officially released recently as the Intel Xeon Processor 5500 Series, is enjoying widespread adoption due to its high-performance and low-power characteristics. It is being deployed in market segments beyond Intel's traditional computer business, such as telecom, military and aerospace, medical, and industrial automation. Designs based on the 5500 Series present several challenges to the older intrusive test technologies, but designers are finding an effective alternative in NBT techniques.

Figure 2 shows a typical circuit board based on the 5500 Series. NBT achieves very high test coverage on this type of board.

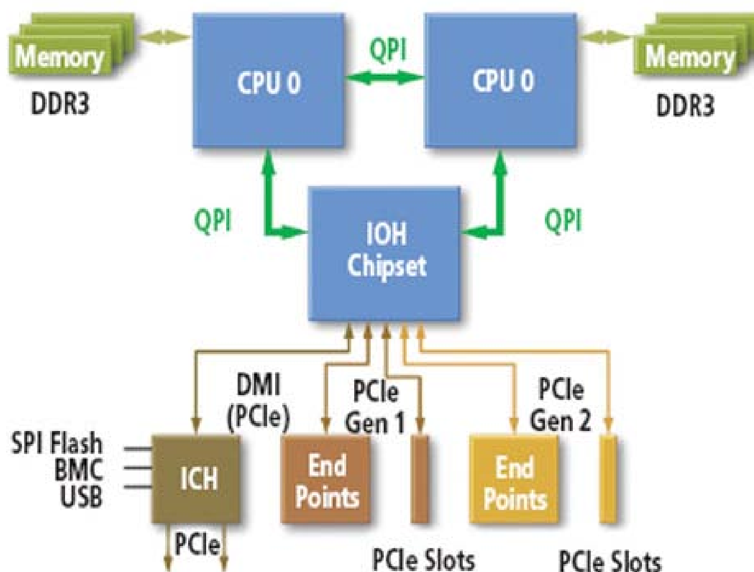

Figure 2. Block Diagram of Xeon Design

Access to the board and chips is provided by a subset of Intel's eXtended Debug Port (XDP), a 60-pin small form factor connector that also is used for general access to current and future Intel silicon, system test resources, and debug facilities. NBT technologies like boundary scan, PCT, and IBIST take up only a small subset of the available XDP signals. In cases where XDP headers are not available, as in high-volume manufacturing, alternatives can be provided.

Boundary scan can provide structural test coverage where it is impossible to insert test pads on the board, such as on the QPI links. If boundary scan is a complementary or supplemental test to intrusive technologies like ICT or flying probe, designing boundary scan into the board will reduce the number of test points on the board. This will dramatically decrease the cost of fixtures for intrusive test. In addition, boundary scan can be used throughout the lifecycle of the system from design and development through manufacturing and field service and repair.

PCT can exercise many of the board's devices and buses with an at-speed functional test, again reducing the need for test points on the board and in fixtures. And because it is a low-level (pre-boot) functional test, PCT will run before the processor's BIOS or operating system has been

loaded. As an at-speed test, it can be applied very quickly when compared to traditional functional tests. Moreover, the diagnostics that accompany PCT are excellent.

Since Intel has included IBIST's embedded instrumentation capabilities in the 5500 Series, IBIST tests and tools also can be deployed. For example, the shape and size of a typical eye diagram generated with IBIST margining tests can validate the design's QPI links without placing a probe on these buses. Other validation tests such as bit error rate routines can be applied to the design nonintrusively through tools that take advantage of the embedded IBIST technology.

Finding Lost Coverage

As technologies advance, disruptive tipping points are inevitable. One type of technology begins to slide away gradually while another takes its place. So it is today with circuit board test and intrusive and nonintrusive test technologies. When obtaining the maximum test coverage possible makes economic sense, the NBT techniques certainly can be deployed in a complementary manner with intrusive technologies like ICT and MDAs. But the ongoing advancement of technology most assuredly points to the incremental ascendance of nonintrusive strategies over time.

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