

Embedded Instrumentation: Its Importance and Adoption in the Test & Measurement Marketplace



A Frost & Sullivan White Paper

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OBJECTIVE AND SCOPE

Solutions for validating and testing current and future generations of printed circuit board (PCB) and chip technologies are evolving in the face of challenges arising from increasing complexities, greater densities, and higher speeds. As a result, an approach known as “embedded instrumentation” is projected to be the future of board and chip level testing. The objective of this White Paper is to analyze the concept of embedded instrumentation and its importance, describe the market trends driving its adoption, and consider the new market entrants in this emerging field.

Frost & Sullivan interviewed leaders in end-market segments, including system manufacturers, semiconductor suppliers, and leading test and measurement (T&M) and EDA vendors. Secondary data was gathered from articles and other sources, including Frost & Sullivan market research.

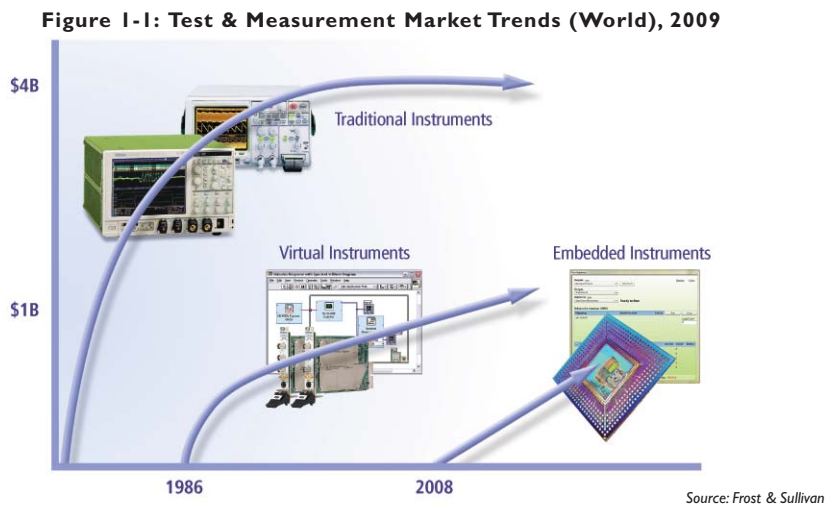
INTRODUCTION

The need for T&M equipment is pervasive for any type of electronic system in virtually all end-user applications, including communications, electronics manufacturing, automotive, industrial, aerospace, military, and others. With board and chip complexity increasing rapidly, it is extremely critical to test for the proper functionality of both the chips themselves and the printed circuit boards (PCB) where they have been installed. For decades now, traditional external instruments have been used to collect and analyze test data. However, it is presently becoming more difficult to use these older types of instruments. The future is about software-based T&M systems and, more generally, embedded instrumentation.

The interface between benchtop T&M equipment and PC-based T&M equipment has been evolving for a considerable period of time. The initial interfacing was provided by parallel and serial interfaces, including the general-purpose interface bus (GPIB). However, the current technological trend requires a more powerful interface, which is provided by implementing universal serial bus (USB), PXI, VXI, and LXI/Ethernet ports.

Embedded instrumentation will also need powerful interfaces for this segment to develop. Industry standards for interfacing to embedded instrumentations are already being developed, and some of these are discussed in this paper, including IEEE 1149.7 and IEEE P1687. These standards build on more established standards like IEEE 1149.1 (JTAG) and IEEE 1500 (Core Wrapper test std.) that will also play key roles in the development of the embedded instrumentation market.

Figure I-1 depicts the major evolutionary trends in the world T&M market.



Traditional Instrumentation

In the past, traditional T&M instrumentation and systems were comprised of pre-defined hardware components that cater to a specific task or kind of analysis. These instruments, such as digital multimeters, oscilloscopes, signal generators, and logic analyzers, have been limited to fixed- or vendor-defined functionality. These conventional instruments are expensive, and upgrades to augment or enhance their functionality only add to their cost and the cost-of-test.

Virtual Instrumentation

Virtual instrumentation is a concept developed in the mid 1980s, which deals with the use of customizable software and modular instrumentation hardware. In essence, virtual instruments are user-defined measurement systems. Certain software packages like National Instruments' LabVIEW are examples of virtual instrumentation.

The major difference between traditional instrumentation systems and virtual instrumentation is the software in the latter, which can be programmed to replace the prescribed hardware functionality of traditional instrumentation. The software of virtual instrumentation assists in reducing the cost of testing by replacing the composite and expensive hardware components in the traditional test systems with a software package. Test-related software, which can capture data and process it for high-speed, real-time analysis, holds the key for the future in the T&M marketplace.

Embedded Instrumentation

Embedded instrumentation is a concept of entrenching and enhancing the capabilities of traditional external test equipment as an additional resource on the chip and/or on

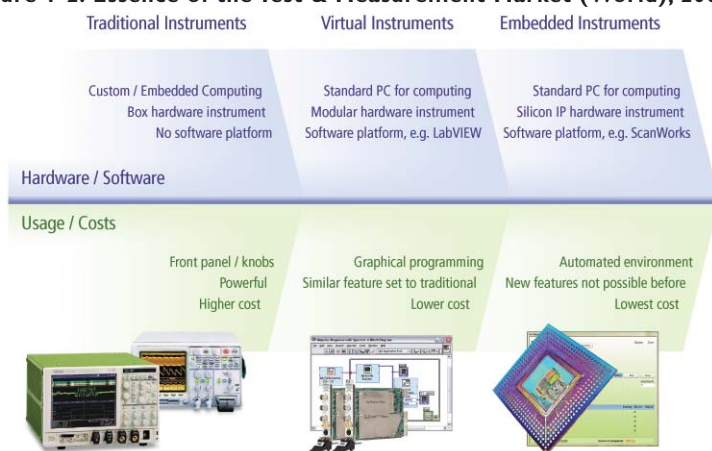
dedicated instrumentation chips on a circuit board. Then, through industry standard access mechanisms, software is used to run the instrument and collect data for analysis.

Since the invention of the integrated circuit, the electronics hardware industry has evolved according to Moore’s law, which asserts that the number of transistors on chips will double every two years. In such a scenario, it is necessary to keep pace with this trend and develop instruments for debugging and testing chips and circuit boards that are faster, denser, and more complex every year. Embedded instrumentation offers an effective solution.

This White Paper is focused on the embedded instrumentation concept that caters to board testing. It will highlight the various solutions currently available in the market to test circuit boards using embedded instrumentation technologies.

Figure 1-2 illustrates how the T&M market has evolved over the past 20 years.

Figure 1-2: Essence of the Test & Measurement Market (World), 2009



Source: Frost & Sullivan

BACKGROUND

Traditional board test technologies can be classified broadly under three main categories, namely:

Validation technologies - Oscilloscopes, logic analyzers, and Bit Error Rate Testers (BERTs),

Inspection technologies - Automated optical inspection/Automated X-ray inspection (AOI/AXI) systems,

Test technologies - In-circuit testers (ICTs), manufacturing defect analyzers (MDA), flying probe testers, boundary scan testers, functional testers, and so on.

Validation Technologies

Various validation tools are typically used to check the operation of any digital system with precision. Each kind of equipment has its own advantages.

- Oscilloscopes

Oscilloscopes are general-purpose test instruments that allow signal voltages to be viewed as a function of time or some other voltage. The main advantages of digital oscilloscopes include the ability to analyze multiple signals associated with intermittent and infrequent events quickly, identify intricate problems by viewing pre-triggered data, and view minute details such as fast glitches, overshoot on pulses, and noise.

- Logic Analyzers

Logic analyzers are electronic instruments that display signals in a digital circuit and are typically used for capturing data in systems that have too many channels to be examined with an oscilloscope. Captured data can be converted into timing diagrams, protocol decodes, state machine traces, or assembly language. Logic analyzers can trigger complicated sequences of digital events and help to capture the digital data from the system-under-test.

- Bit Error Rate Tester (BERT)

A BERT is used in various fields, such as digital circuits, mobile communications, digital broadcasting, and even in field testing for the examination of bit error rate (BER) and error frequency. It tests a physical data interface by transmitting and receiving data through that interface. The BER is defined as the percentage of bits with errors relative to the total number of bits transmitted. It is usually expressed as 10 to a negative power.

In a high-speed serial I/O test, oscilloscopes are used to test transmitters. Such a test consists of a circuit transmitting a pre-defined signal while the oscilloscope measures it. While oscilloscopes monitor physical-layer signals, logic analyzers are used to examine logical information and to trace information from protocol data flow. BERTs are specifically confined to high-speed I/O testing.

Inspection Technologies

- Automated Optical Inspection

AOI is an automated visual inspection technology for a wide range of products, such as PCBs, liquid crystal displays (LCDs), transistors, automotive parts, lids and labels on product packages, and agricultural products. AOI is a non-contact type of white box testing commonly used in the manufacturing process.

- Automated X-ray Inspection

AXI is a technology based on the same principles as AOI, except that X-ray technology is employed by AXI instead of visible light sensors. AXI inspects features which are typically hidden from view. AXI plays a major role in testing integrated circuits (ICs) with packages such as ball grid array (BGAs), where the connections are hidden underneath the chip, making optical inspection impossible.

Test Technologies

- In-circuit Test

In-circuit test (ICT) is one of the most prevalent types of board-level test technologies for electrical tests. It involves a bed-of-nails (BON) test fixture, which makes connections to various test points or pads on the PCB for the purposes of performing structural electrical testing of the board's circuits.

- Boundary Scan Test

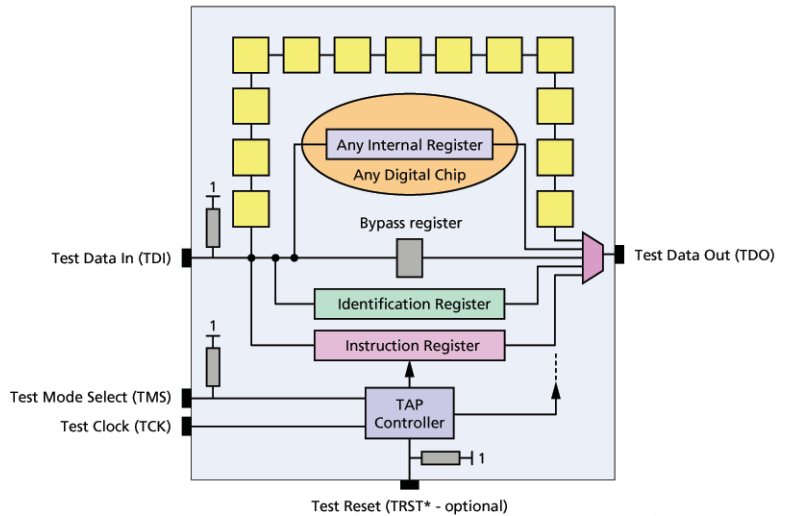
Boundary scan is defined by the IEEE 1149.1 standard. It is a method for testing interconnects among ICs on PCBs. The boundary scan standard is sometimes referred to as JTAG after the Joint Test Action Group, which initiated its development. Moreover, the term JTAG often refers to the access interface on chips as defined by the IEEE 1149.1 standard. Since its inception in the early 1990s, the IEEE 1149.1 standard has become more prevalent, especially in the telecommunication and defense/avionics industries. Some of the key advantages of the boundary scan test are the following: (1) it solves the problem of the lack of access to test points as experienced by ICT, (2) it has shorter test times than ICT, (3) it achieves higher test coverage, (4) it offers enhanced diagnostic capabilities, and (5) its capital equipment costs are much lower than ICT and other intrusive test technologies.

In the manufacturing process, a boundary scan test can first be deployed to debug, test, and diagnose circuit board prototypes. It is typically used to check the electrical continuity of the interconnections of chips on a circuit board. One of its key benefits is the access it provides to components and circuitry inside a PCB, thereby enabling tests that would otherwise be impossible to perform with probe-based technologies.

Boundary scan testing is an effective complement to other techniques, such as ICT and functional test, when they are not sufficient by themselves to perform a satisfactory test of circuits on the PCB under test. The IEEE 1149.1 Boundary Scan Standard has become a standard part of most companies' circuit board testing methodologies, and, in particular, it has been accepted as one of the best tests for compact and complicated electronics units.

Figure 1-3 illustrates the IEEE 1149.1 architecture at the chip level.

Figure 1-3: IEEE 1149.1 Chip Architecture



Source: Frost & Sullivan

- Functional Test

Functional testing attempts to verify the functionality of an entire PCB. It combines both general-purpose and application-specific test functionalities. Although functional test systems offer the potential of high pass/fail fault coverage and accurate test results, diagnosing root causes of failures can be very costly. For example, when failures are reported by a functional test, identifying the exact nature and location of the fault is very difficult and time consuming. This can drive up test costs significantly. In addition, high-level technical skills are required to maintain a functional test strategy and to interpret its results.

TECHNICAL DISCONTINUITIES

All the above-mentioned technologies for validation, inspection, and test have been successful to a certain extent. However, with the current complex nature of boards and chips, it is becoming increasingly difficult to perform tests effectively and efficiently. Several technical discontinuities are emerging from testing new highly integrated chips and complex boards. Current test technologies, as discussed above, are losing their effectiveness due to this additional complexity. Various deficiencies lead to difficulty in measuring and gathering data using the technologies mentioned above. Some of the complicating factors include the following:

- Lack of test access for PCB structural testing
- Lack of test access for signal integrity testing
- The migration to chip interconnects speeds in excess of 5 gigabits per second (Gbps)

- The need for protocol-aware, high-speed I/O test
- Limited capacity of testers

Lack of Test Access for PCB Structural Testing

Exponentially increasing levels of board and chip integration are rendering legacy intrusive structural test technologies obsolete. The number or mere presence of test points on PCBs, which would enable the use of intrusive probe-based testers, has been severely limited and reduced over time. This has challenged electronics manufacturers that are continually trying to increase the features of next-generation product while, at the same time, minimizing the size of circuit boards. Due to the increased densities of boards, it has become increasingly difficult to probe the electronic circuits on these boards to gather the required test information.

Lack of Test Access for Signal Integrity Testing

Access to on-board, chip-to-chip signals is diminishing because probes placed on these interconnects distort the signals. As a result, accurate tests are becoming increasingly difficult to perform. Many test solution providers mathematically model external probes so as to remove the effects that real physical probes have on signals. These modeling exercises extrapolate what the “true” test data would be from a real physical probe. However, it is unclear how deterministic this approach will be as I/O speeds become increasingly faster and as quantum-mechanical effects become more pronounced.

The accessibility issue is becoming more severe with the complex nature of chips and high-speed serial data signals. To test hard-to-access signals inside boards and on chips, embedded instrumentation is a key enabling technology.

The Migration to Chip Interconnects Speeds in Excess of 5 Gigabits per second (Gbps)

As the speed of the signals on interconnects that link chips on circuit boards increases, there is a greater chance that the signals will be distorted when a physical test probe is placed on the interconnect. Gathering accurate test data on an interconnect is difficult when that data is distorted by a probe. This has resulted in vendors being forced to develop and deploy costlier probes, which may not be as effective, but which increase the cost of the entire test system. As serial data speeds increase, so does the cost of testing. Also, accuracy of the reconstructed waveform data using transformation and simulation techniques becomes more problematic as speeds increase. For example, at multi-gigabit speeds, Heisenberg’s Uncertainty Principle, which states that position and momentum of an electron cannot both be known to arbitrary precision, will have a significant effect.

With capital expenditure (CAPEX) being a key issue as a result of the global economic downturn, test equipment vendors face a challenge to offer sophisticated, cost-effective

solutions. As the speed of signals increases, design-for-test complexities also multiply. Moreover, issues relating to the accessing of data challenge test systems at these speeds. Designers need to be able to plan for these challenges by making inroads to reach the data points and retrieve signals during testing. The complex nature of boards and chips is making it more difficult to test and points out the need for new testing standards.

Table I.1 illustrates the increasing speeds of standard buses and chip interconnect technologies.

Table I-1: Interconnect Standards and Specifications (World), 2008

Standard Busses	Speed (Gbps or GT/s)	Initial Adoption
PCI Express I	2.5	2002
PCI Express II	5.0	2008
PCI Express III	8.0	2010
Serial ATA I	1.5	2002
Serial ATA II	3.0	2005
Serial ATA III	6.0	2009
USB 1.0	0.012	1996
USB 2.0	0.480	2000
USB 3.0	4.8	2008
XAUI	3.125	2005
Intel QPI	6.4	2008
HDMI 1.0	4.9	2002
HDMI 1.3	10.2	2006

Source: Frost & Sullivan

The Need for Protocol-Aware, High-Speed I/O Test

In many new chip and ASIC designs, the upper layers of the Open System Interconnection Reference Model (OSI Model) are encapsulated within silicon in order to more effectively perform packet management and quality-of-service (QoS) classification for file transfer protocol (FTP), hypertext transfer protocol (HTTP), packetized voice and video, and other forms of packetized data traffic. For certain chip-to-chip serial interconnects, such as PCI Express, XAUI, Intel QuickPath Interconnect (QPI) and others, protocol-level validation is needed in addition to physical-layer framing and data integrity testing. That is, it is no longer acceptable to test solely at the physical layer in order to confirm the functional performance of a working system. In this domain, the cost of external test equipment becomes prohibitive because no legacy test system can test multiple OSI levels on multiple lanes on a multi-gigabit link in an integrated fashion. In contrast to the deficiencies of legacy test technologies, software-based embedded instrumentation can perform transport- and even session-aware testing.

Limited Capacity of Testers

It is becoming increasingly difficult today for a tester to exercise all of the signals on a large PCB simultaneously. In addition, traditional external instruments are limited in their

capacity to trace a large number of signals simultaneously. This has significant implications on the information obtained from tests and extends the time required for tests, which drives up test costs. In addition, effects that may be experienced in the field, such as high CPU I/O processing simultaneous with high memory traffic, cannot be replicated in the lab with legacy testers. This can increase a product's "time to market" significantly at a time when vendors face challenges to reduce a new system's development time and accelerate the product's life cycle. Also, quality issues in the field, such as high levels of No Trouble Found (NTF) problems, increase the cost of warranty returns and lead to customer dissatisfaction.

Summary of Challenges and Costs

As electronic products become miniaturized, it becomes increasingly difficult to perform testing on smaller boards and more highly integrated chips. In addition, as on-board signal speeds increase, testing becomes more expensive and challenging. Due to increasing bus speeds and complexities, the usefulness of traditional approaches diminishes, thereby forcing engineers to consider a broader range of solutions for the immediate future. Performing real-time, at-speed testing is a major difficulty because it is very challenging to analyze the actual test data from the system. In many cases, the only option to increase testability is to redesign the circuit board with test in mind.

Currently, manufacturers do not want to spend more money on tests unless they experience an inescapable need for it. To satisfy the greater demands for improved test coverage that manufacturers are placing on their test systems, providers of legacy- and probe-based test systems have built new testers. These testers are more costly, yet they often do not return the results expected. Hence, by increasing test accessibility and adding value to the manufacturing process, embedded instrumentation is likely to assist the growth of testers and test vendors.

EMBEDDED INSTRUMENTATION – SOLVING VALIDATION, TEST, AND DEBUG PROBLEMS

Embedded Instrumentation – What is it?

Embedded instruments are IP inserted within chips to perform specific validation, test, and debug functions. These functions can relate to silicon validation and test, or they can be used to functionally or structurally exercise a printed circuit board or an entire system.

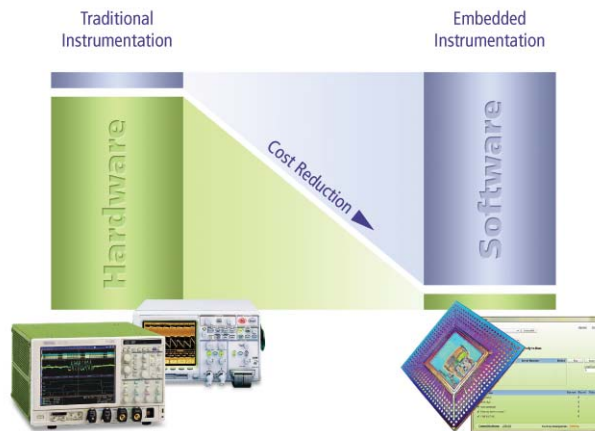
Embedded instruments have been around for a long time. Many semiconductor suppliers support dozens or even hundreds of test instruments within their silicon. These instruments range from built-in oscilloscopes, logic analyzers, memory built-in self test (MBIST), power meters, temperature monitors, a variety of sensors, and so on. Typically, these instruments are only exposed within the silicon characterization and validation lab of the chip supplier. More recently, the forward-thinking chip suppliers have been making many of these instruments accessible to their users, the printed board designers, and system

manufacturers. This is done in the spirit of helping their users improve the quality of their products. Some examples of this embedded instrumentation include Intel®'s Interconnect Built-In Self Test (IBIST) for QuickPath Interconnect (QPI) and PCIe BERT/margining, and PLX Technology's visionPAK™ PCIe packet generator/analyzer toolkit.

As these embedded instrumentation IP modules are meant to be used non-intrusively within a working printed circuit board, access to the instruments is done via a “soft” connection, typically the chip's JTAG test access port (TAP). For reasons described earlier in this White Paper, this accrues all of the benefits of eliminating external test access points. For the board designer, it is a simple matter of ensuring that the targeted chip's JTAG TAP is accessible to external software. The targeted device can easily be put into a chain of other devices on the board and become the target of software-based boundary scan, processor-controlled test, and/or BIST-type test applications. This type of embedded instrumentation test strategy for a circuit board lends itself to test solutions that are much less hardware-intensive than in the past and, therefore, far more cost-effective, agile, and flexible.

Figure I-4 depicts the traditional test methods versus embedded instrumentation test/validation.

Figure I-4: Traditional versus Embedded Instrumentation Architecture (World), 2009



Source: Frost & Sullivan

Some of the test technologies that utilize embedded instrumentation include boundary scan test, processor-controlled test, I/O instrumentation test and core instrumentation test. Some of the embedded instruments that reside within chips/boards and the applications that use them are briefly described below.

Boundary Scan

Boundary scan test has been used since the early 1990s, and is accepted as a fundamental embedded instrumentation technology and as a very effective tool for structural fault coverage. The IEEE 1149.1 Boundary Scan Standard was initially developed to test the

electrical continuity of the interconnections between ICs on boards, modules, and other substrates. Further enhancements were made, including the boundary scan description language (BSDL), which enabled boundary scan tests to be written in a common language. As the original IEEE 1149.1 standard caters only to testing DC-coupled, single-ended networks, several new standards have been developed that utilize the chip- and board-level IEEE 1149.1 infrastructure that has been embedded in chips and on circuit boards. For example, the IEEE 1149.6 standard is based on IEEE 1149.1 but it applies to the testing of high-speed, AC-coupled interconnects among chips on a circuit board, something that the original IEEE 1149.1 boundary scan standard cannot test. This new IEEE 1149.6 standard extended the capabilities of the basic boundary scan standard (IEEE 1149.1) to include AC-coupled and differential nets on a circuit board. The 1149.6 standard was approved in March 2003, and since then it has witnessed some limited success. However, not all serializer/deserializer (SerDes) chips support the IEEE 1149.6 standard.

Several other emerging standards have also been built on the foundation laid by the IEEE 1149.1 Boundary Scan Standard. At least two of these standards are expected to have a major affect on the adoption and efficient use of embedded instrumentation in the industry.

The IEEE 1149.7 standard defines a next-generation TAP while maintaining backward compatibility with the original four-wire IEEE 1149.1 TAP to take advantage of the installed base of 1149.1 technology. The primary goal of this standard was to be compatible with existing IEEE 1149.1 systems but operate with fewer pins. This standard, also known as “two-wire JTAG,” compact JTAG, or cJTAG, is expected to become an important tool for testing multi-chip modules, 3D stacked die packages, and so on in the future. IEEE 1149.7 was recently ratified and approved.

Another emerging standard also utilizes the original IEEE 1149.1 boundary scan standard. The IEEE P1687 is a standard for the control and management of embedded instrumentation within a semiconductor device with application to board test. This standard offers advantages such as simplified routing and a standard interface. Once established, P1687 is expected to offer greater functionality for test by using embedded instrumentation. Potential users also opine that new standards such as IEEE 1149.7 and IEEE P1687 are the key to the future growth of the embedded instrumentation test equipment market.

Processor-Controlled Test

On any given design, the most powerful instrument is the processor. Whether it is within a System-on-a-Chip (SoC) or a PCB, the processor typically has the ability to exercise all subtending memory and I/O. It does this via an “embedded instrument” called its debug port, by which it can be reset and used to run dedicated test code. This approach, commonly called processor-controlled test (PCT), takes advantage of the very low-level control that a CPU has over the devices it is connected to on a PCB. Thus, this technology is known for extremely high levels of test coverage combined with very granular diagnostics and fault isolation. The trade-offs are typically the overhead necessary to create and

maintain the test code, which is often written in assembler or low-level “C” code. However, some test solutions on the market, such as ASSET® InterTech’s ScanWorks® with PCT, abstract the specifics of the hardware from the test engineer and support higher-level language access to the CPU debug port, thereby making this a very cost- and time-effective solution.

I/O Instrumentation

I/O instrumentation relates to a subset of embedded instrumentation which is used to validate and test high-speed I/O links. Examples of these are Intel® IBIST and PLX visionPAK™. These instruments can operate at the physical layer, or they can climb the stack and become transport and protocol aware. Currently, many devices (Intel, Avago, PLX, and others) and I/O IP (Snowbush, Synopsys, Mentor, and others) include test IP for applications like BERT and margining to aid in PCB signal integrity validation.

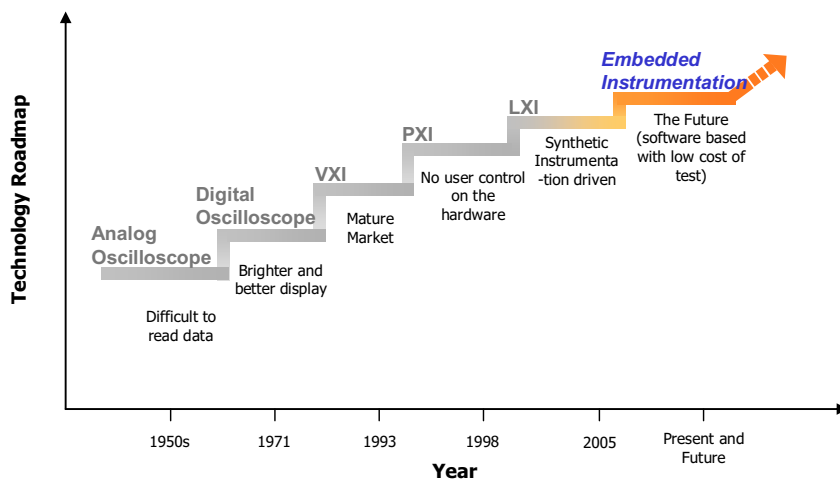
Core Instrumentation

Core instrumentation relates to the more generalized manifestation of embedded instrumentation for the purposes of chip and board validation, test, and debug.

The foundation of core instrumentation is IEEE P1687, which is expected to be ratified in the second half of 2010. IEEE P1687 specifies a standardized method of access and control for embedded instrumentation. Already enjoying a certain degree of implementation in the industry prior to the ratification of the standard, this technology will have far-reaching effects on new test solutions.

Figure I-5 illustrates the technology evolution timeline since the 1950s.

Figure I-5: Technology Evolution Timeline (World), 1950-Present



Source: Frost & Sullivan

MARKET TRENDS

Boundary scan testing is used globally. Several small and regional companies have emerged with niche boundary scan test solutions. However, these do not form the sophisticated, automated type of test solutions that are offered by the key vendors in this market segment -- ASSET InterTech (United States), GOEPEL Electronic (Germany), and JTAG Technologies (Netherlands). This environment of upcoming companies brings more exposure to the IEEE 1149.1 standard, and it is expected to boost the growth of boundary scan testing in the future. With embedded instrumentation adding more value to the boundary scan infrastructure on circuit boards and in chips, it is very evident that the JTAG accessibility provided by the boundary scan standard will make testing more viable and successful over time.

A critical factor that accelerates the adoption of emerging technologies is the support they receive from open industry standards, such as those developed and promulgated by IEEE, JEDEC, and other industry bodies. Beginning with the development of the original IEEE 1149.1 Boundary Scan Standard, embedded instrumentation has received excellent support from an array of standards. Moving forward, several standards in the final stages of adoption hold great promise for opening new areas to embedded instrumentation while delivering more efficient and effective validation and test results to manufacturers.

Taken together, these two emerging standards, IEEE 1149.7 and IEEE P1687, will have great advantages for the use of embedded instrumentation in the near future. For example, both of these standards could be applied with benefit to using embedded instrumentation to test and validate 3D multiple-die chip packages, which some predict will soon become a prevalent technology and allow the industry to keep up with Moore's law in the future.

The IEEE 1149.7 standard is particularly adaptable to through-silicon via (TSV), which is essential for 3D die stacked chips. Architectural enhancements to IEEE 1149.7 over IEEE 1149.1 also make it effective for testing and validating 3D chips. With access provided to embedded instrumentation by IEEE 1149.7 and IEEE 1149.1, the IEEE P1687 standard can manage and control those instruments. IEEE P1687 can be critical to automating the operation of embedded instruments to facilitate the correlation of their test results.

Design-for-test (DFT) plays an important role in the testing business as well. It is highly critical to ensure that the circuit boards and chips are designed according to the requirements of various tests that the UUT will undergo. The complex nature of these boards and chips requires more in-depth knowledge of DFT principles, but, in the long run, DFT reduces the cost of testing.

The problem of test accessibility is significant, and conventional intrusive test methods with probes, such as ICT, are becoming less effective because their access is eroding. Every test technology such as ICT, boundary scan testing, and functional test has its limitations. These limitations augment as chip density increases. In such a scenario, embedded instrumentation

will play a key role in the near future. Currently, semiconductor vendors need to work with board hardware design engineers to alter/modify chip designs to enable better validation and test control. Despite the fact that ICT is not expected to be totally replaced on manufacturing lines in the near future, several companies are moving toward boundary scan testing and other non-intrusive technologies to enable better testing of the board and IC circuitry.

A key concern for manufacturers is keeping up with new technologies because this provides them with their competitive advantage. The key factors for test vendors to succeed in this market are to provide powerful test capabilities with an easy-to-use interface, and hardware and software support with a favorable price-to-performance ratio. Many of today's instruments used for test and validation pertain to the lab environment, but the future is focused on developing key solutions to operate in the manufacturing environment as well.

MARKET ANALYSIS

Validation Technologies

According to Frost & Sullivan research, the oscilloscopes market witnessed product launches via bandwidth updates in late 2008 and early 2009. The digital oscilloscopes market registered revenues of \$1,176.8 million in 2008. The average price of the high-end oscilloscopes ranges between \$150,000 and \$250,000, depending on the bandwidth and other ingredients available with the package. The leading market participants in this segment include Tektronix, Inc., Agilent Technologies, LeCroy Corporation, Yokogawa Electric Corporation, National Instruments, Fluke Corporation, Pico Technology, VXI Technology, Geotest Marvin, ZTEC Instruments, Iwatsu Test Instruments Corporation, Good Will Instrument Co., Ltd., EZ Digital, Rigol Technologies Inc., Hameg Instruments, and so on. This market is expected to grow at a compound annual growth rate (CAGR) of 6.0 percent from 2008 to 2013.

Similarly, Frost & Sullivan estimated the logic analyzers market revenues to be \$232.0 million in 2008, which was represented by a decline of negative 0.2 percent from that of the previous year in 2007. The average prices of these products are approximately \$14,500. The major market participants include Tektronix, Inc., Agilent Technologies, Inc., Good Will Instrument Co., Ltd., and Thurlby Thandar Instruments Ltd., among others. The growth of this market has been impacted by the signal generators market and is expected to grow at a CAGR of 0.2 percent from 2008 to 2013.

The BERT market generated revenues of approximately \$365.0 million in 2008, according to Frost & Sullivan research analysis. BERT prices range from \$2,000 to \$165,000, depending on whether it is a low handheld type or a high-performance, next-generation tester. The BERT market is expected to grow approximately at a CAGR of 5.0 percent. The key market participants in this segment are Agilent Technologies, JDS Uniphase Corporation, Anritsu Corporation, Sunrise Telecom Incorporation, Advantest Corporation, Spirent Communications, Aeroflex Incorporated, SyntheSys Research, Inc., Ixia, and other small regional companies.

Test Technologies

The ICT market was found to be \$354.7 million in 2008, growing at the rate of 4.7 percent from that of the previous year. The growth rates are expected to decelerate at a slow pace during the forecast period due in part to other test technologies taking share from this segment. One of the main reasons for the deceleration in growth in this segment is the increasing complexity of PCBs, which makes it difficult for in-circuit testers to access the test points in the circuit boards.

The revenues generated by the functional test market were \$628.9 million in 2008. Functional testers are product-specific, and the growth of this market segment depends on the growth of its respective end-user industries.

In 2008, the revenues generated by the manufacturing defect analyzer (MDA) tester market were \$130.7 million. This was a growth of 5.3 percent from that of the previous year. The growth rate of this market segment is relatively flat.

The boundary scan testing equipment market registered revenues of \$28.8 million in 2008, which was an increase of 8.6 percent from that of the previous year. The CAGR is expected to be 8.5 percent from 2008 to 2013. The top three vendors in this market include ASSET InterTech (United States), GOEPEL electronic (Germany), and JTAG Technologies (Netherlands). North America contributed 46.0 percent of the market revenues in 2008, followed by Europe, Asia Pacific, and Rest-of-World with 38.5, 11.5, and 4.0 percent, respectively.

From the above analysis, it is evident that the boundary scan test market is expected to grow the fastest among all types of legacy test technologies. In addition, the cost of boundary scan ATE is estimated in the range of \$10,000 to \$40,000, starting with manufacturing run-time capabilities and going to fully configured boundary scan test development systems. For comparable capabilities, boundary scan test is much less expensive than the older probe-based test technologies. This is due to the fact that boundary scan testers are more software-oriented.

As more instruments are embedded into chips and as more embedded instrumentation test technologies are implemented, these factors will dramatically accelerate the growth of companies like ASSET, which have chosen to focus on embedded instrumentation as a key enabler for more efficient and effective board and chip test in the future.

CONCLUSIONS

With CAPEX being a key issue in the downturn-affected market and into the future, hardware design and manufacturing companies in the electronics industry prefer low-cost, high-value test equipment. Software-based test instruments are gaining more value compared to their traditional hardware-oriented counterparts, and this trend is increasing on a day-to-day basis. In addition, these software-oriented test technologies require

software upgrades with minimal hardware, which, in turn, reduces the cost of advanced systems with new technologies.

When access to chips is more feasible by way of the JTAG port on chips and other access technologies, the concept of embedded instrumentation becomes more effective for testing circuit boards, as well as chips like microprocessors, DSP chips, FPGA, and others that are on boards. As time is crucial, effective and efficient testing of PCBs is critical. Through embedded instrumentation, and the use of the JTAG port on chips for access and the boundary scan infrastructure on circuit boards, this can be achieved, and this is expected to be the future of PCB testing. Thus, the concept of embedded instrumentation helps improve the quality of chips, circuit boards, and the systems where they are installed.

The key factor for success in the PCB testing market is to provide ease-of-use with flexibility. Price-to-performance ratio is also another key factor, which lures manufacturers to purchase a particular type of test technology from a vendor. Embedded instrumentation is expected to have the potential advantages of effective and efficient testing of complex circuit boards, shorter test times, higher test coverage, increased diagnostic capabilities, and lower capital equipment cost. This will improve the price-to-performance ratio of many types of products like consumer electronics, avionics, computers, defense systems, telecommunications, and others.

As CAPEX continues to be a critical issue, system manufacturers will require more efficient testing, and there is expected to be more development in IEEE standards to support testing in the future. In the high-speed serial I/O market specifically, there is expected to be more growth of new technologies and diminishing use of traditional test equipment.

Research indicates that testing utilizing embedded instrumentation will essentially use the JTAG IEEE 1149.1 access port on chips as a gateway standard, and other standards will emerge to get access to circuit boards and the chips on them by non-invasive methods during PCB validation and testing. There is expected to be a transfer from external instrumentation to internal embedded instrumentation, which will be stimulated by standards such as IEEE P1687 and IEEE 1149.7, for example.

Frost & Sullivan will continue to track the development of the embedded instrumentation market. We will continue to add more specific market size projections, as these relate to the adoption of embedded instrumentation technology by electronic manufacturers in our test and measurement market reports in the future.

ACRONYMS

AOI/AXI – Automated optical inspection/Automated X-ray inspection
ATE – Automated test equipment
BERT – Bit Error Rate Tester
BGA – Ball grid array
BIST – Built-in self-test
BON – Bed of nails
BSDL – Boundary Scan Description Language
CAGR – Compound Annual Growth Rate
CAPEX – Capital expenditure
CPU – Central processing unit
DFT – Design for test
FPGA – Field-programmable gate array
FTP – File Transfer Protocol
Gbps – Gigabits per second
GPIB – General-purpose interface bus
GT/s – Giga Transactions per second
HDMI – High-definition multimedia interface
HTTP- Hypertext Transfer Protocol
IBIST – Interconnect Built-In Self Test
IC – Integrated circuit
ICT – In-circuit test
IP – Internet Protocol
IEEE – Institute of Electrical and Electronics Engineers
JTAG – Joint Test Action Group
LXI – LAN eXtensions for instrumentation
MDA – Manufacturing defect analyzer
MIPI® – Mobile Industry Processor Interface
NTF - No trouble found
OSI Model – Open System Interconnection Reference Model
PCB – Printed circuit board
PCT – Processor-controlled test
PXI – PCI eXtensions for instrumentation
SiP – System-in-package
SoC – System-on-chip
T&M – Test and measurement
TAP – Test access port
USB – Universal serial bus
UUT – Unit under test
VXI – VME eXtensions for instrumentation
XAUI – Extended Auxiliary Unit Interface

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